Digital Forensic Engineering

- Digital Watermarking
- False claim of Ownership
- Computational Forensic Engineering (CFE)
- IP Overbuilding
- Piracy
- IP metering
- Trojan Insertion
- Logic Obfuscation

Intellectual Property - Core Security

IEEE VLSI Circuits & Systems Letter
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IEEE VLSI Circuits and Systems Letter (VCAL) - TCVLSI

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The VLSI Circuits and Systems Letter (VCAL) is affiliated with the Technical Committee on VLSI (TCVLSI) under the IEEE Computer Society (https://www.computer.org/web/tcvelsi/editorial-board). It aims to report recent advances in VLSI technology, education and opportunities and, consequently, grow the research and education activities in the area. The letter, published quarterly (from 2018), covers the design methodologies for advanced VLSI circuit and systems, including digital circuits and systems, hardware security, design for protection, analog and radio-frequency circuits, as well as mixed-signal circuits and systems. The emphasis of TCVLSI falls on integrating the design, secured computer-aided design, fabrication, application, and business aspects of VLSI while encompassing both hardware and software.

TCVLSI sponsors a number of premium conferences and workshops, including, but not limited to, ASAP, ASYNC, ISVLSI, IWLS, SLIP, and ARITH. Emerging research topics and state-of-the-art advances on VLSI circuits and systems are reported at these events on a regular basis. Best paper awards are selected at these conferences to promote the high quality research work each year. In addition to these research activities, TCVLSI also supports a variety of educational activities related to TCVLSI. Several student travel grants are sponsored by TCVLSI in the following meetings: ASAP 2018, ISVLSI 2018, IWLS 2018, iSES 2018 (formerly iNIS 2017) and SLIP 2018. Funds are provided to compensate student travels to these meetings as well as attract more student participation. The organizing committees of these meetings undertake the task of selecting right candidates for these awards.

This issue of the VLSI Circuits and Systems Letter highlights Joseph Cavallaro, IEEE Fellow at Rice University, USA, as our “Feature Member”. It also showcases the state-of-the-art developments covering several emerging areas: hardware security, low-power and robust circuit design and test, emerging devices and circuits, etc. The central theme of this issue is on ‘Hardware Security and Protection’. Professional articles are solicited from technical experts to provide an in-depth review of these areas. The articles can be found in the section of “Features Articles”. In the section of “Updates”, upcoming conferences/workshops, call for papers and proposals, funding opportunities, job openings and Ph.D. fellowships are summarized.

We would like to express our great appreciation to all editorial board members (Yiyu Shi, Shiyan Hu, Hideharu Amano, Mike Borowczak, Helen Li, Himanshu Thapliyal, Michael Hübner, Theocharis Theocharides, Saket Srivastava, Yasuhiro Takahashi, Jun Tao, Sergio Saponara and Qi Zhu) for their dedicated effort and strong support in organizing this letter. The complete editorial board information is available at: https://www.computer.org/web/tcvelsi/editorial-board. We are thankful to our web chair Mike Borowczak, for his professional service to make the letter publicly available on the Internet. We wish to thank all authors who have contributed their professional articles to this issue. We hope that you will have an enjoyable moment when reading the letter! The call for contributions for the next issue is available at the end of this issue and we encourage you to submit articles, news, etc. to an associate editor covering that scope.
Feature Member

Dr. Joseph R. Cavallaro
Professor, Electrical and Computer Engineering
Professor, Computer Science
Director, Center for Multimedia Communication

Joseph R. Cavallaro (S'78, M'82, SM'05, F'15) is a Professor in the Electrical and Computer Engineering Department at Rice University, Houston, Texas. He is also currently Director of the Rice Center for Multimedia Communication, and Associate Chair of the Department of Electrical and Computer Engineering at Rice. He holds a joint appointment in the Department of Computer Science at Rice and is a Docent in the Centre for Wireless Communications at the University of Oulu in Finland. His educational background includes a B.S. in Electrical Engineering from the University of Pennsylvania (1981), an M.S. in Electrical Engineering from Princeton University (1982) and a Ph.D. in Electrical Engineering from Cornell University (1988). He has been engaged in research since 1981 after joining AT&T Bell Laboratories as a Member of Technical Staff and his research interests include VLSI signal processing with applications to wireless communication systems.

At the Rice Center for Multimedia Communication, his research is on multiple antenna systems (MIMO), with a focus on baseband signal processing for beyond 5G wireless systems. Current topics include parallel VLSI architectures for iterative detection and decoding, in particular, architectures for soft sphere detection and low density parity check codes (LDPC), along with massive MIMO systems. These high performance receiver algorithms will provide more reliable higher data rate communication systems and are being investigated in over the air testing on the Rice Wireless Open-Access Research Platform (WARP). His research interests include algorithms, architectures, and implementation for computer arithmetic and VLSI signal processing including applications of CORDIC arithmetic and ASIC, FPGA, and GPU systems.

Prof. Cavallaro has received honors and awards including IEEE Circuits and Systems Society Distinguished Lecturer (2012-2013), Nokia Foundation Visiting Professor Fellowship (2004), IEEE Computer Society Distinguished Visitor (2004-2006), Hershel M. Rich Invention Award (Rice Engineering Alumni, 1994), National Science Foundation Research Initiation Award (1989-92), IBM Graduate Fellowship (1987-88), and a National Merit Scholarship (1977-78). He has published over 50 journal articles and over 150 conference articles, book chapters, and technical reports, and has received several best paper awards, including at the 2009 ACM/IEEE Great Lakes Symposium on VLSI, the 2008 IEEE System on Chip Conference, and the 2008 IEEE Workshop on Signal Processing Systems. Prof. Cavallaro has been awarded 10 patents with 11 pending related to his academic research. The National Science Foundation and the State of Texas have supported his research along with Nokia, Nokia-Siemens Networks, Renesas Mobile Europe, Texas Instruments, Huawei, Xilinx, Samsung Telecommunications, and National Instruments. Cavallaro has served as a Technical/General Co-Chair for 8 ACM and IEEE conferences and a program committee member and/or session chair for over 15 conferences, He has graduated 19 Ph.D. students, and has served on thesis committees for many others, including serving as an External Referee / Thesis Committee Member / Opponent on Ph.D. thesis committees at the Indian Institute of Technology, the Royal Institute of Technology (KTH), Sweden, Linköping Univ., Sweden, Tampere Univ. of Technology, Finland, and Queen’s University, Belfast, N. Ireland. During 1996-97, Prof. Cavallaro served as a Program Director at the US National Science Foundation (NSF) in the Systems Prototyping and Fabrication Program in the Microelectronic Information Processing Systems Division responsible for research support in computer systems prototyping and VLSI Design through MOSIS. During the

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spring of 2005, he was a Nokia Foundation Fellow and a Visiting Professor at the Centre for Wireless Communications at the University of Oulu in Finland. He is the past chair of the IEEE Computer Society Technical Committee on VLSI. He chairs the IEEE Houston Chapter of the Circuits and Systems Society, is the IEEE Rice University Student Branch faculty counselor, and is a member and Chair-Elect of the IEEE CAS Circuits & Systems for Communications Technical Committee and an advisory board member of the IEEE SPS Design and Implementation of Signal Processing Systems Technical Committee. He is currently an Associate Editor for the Spring Journal of Signal Processing Systems, the IEEE Signal Processing Letters and the IEEE Transactions on Signal Processing. He is serving as the IEEE Circuits and Systems Society Representative to IEEE-USA's Research & Development Policy Committee (R&DPC) and was a Member of the Board of Governors of the IEEE Circuits and Systems Society. Prof. Cavallaro is a member of ACM and an IEEE Fellow for contributions to very large-scale integration (VLSI) architectures and algorithms for signal processing and wireless communications. For further information on research and publications, please see: http://www.ece.rice.edu/~cavallar and http://warp.rice.edu.

Q1. Tell us a little about your research area and what motivated you to get into it?

My research is in the area of VLSI signal processing with a broad variety of applications from robotics to wireless communications to recently, healthcare. My work has included the integration of algorithms and architectures to build systems. Parallelism and the analysis of computational complexity and reliability have been important features. In my graduate work in the 1980's I was attracted to the parallelism that could be achieved with systolic arrays. However, efficient implementation was essential in the early days of VLSI and that drew me to investigate interesting computer arithmetic algorithms. In particular, CORDIC arithmetic for hardware calculation of sine, cosine, and inverse tangent was emerging as an important method. My research on systolic arrays for the Singular Value Decompositions (SVD) using CORDIC arithmetic was my first major contribution that has had applications in direction of arrival in radar and sonar, inverse kinematics in robotics, channel estimation in wireless communications, and in machine learning.

Q2. What are some of your proudest accomplishments?

I am pleased to have contributed to research, education, and the technical community in VLSI. I am proud to have educated hundreds of students in VLSI design through the years who are making enormous contributions in industry and academia. I have been fortunate to have had excellent PhD students who have made many advances in algorithms and architectures in applications from robotics to wireless communication systems. Our research has been supported by the NSF, DOE, and many communications and computer companies. In the 1990's we collaborated with Sandia National Labs and the DOE on fault tolerant robotic control systems for a critical safety application. These real-time fault tolerant system architectures were created for robotic systems for hazardous waste cleanup planned for remediation of leaking nuclear waste storage tanks. Over the last 20 years, I have made contributions to the algorithms, architectures, and VLSI implementations of the physical layer signal processing of 3G, 4G, and current 5G wireless communication systems. Many of our papers and patents for multiuser detection, sphere detection, and turbo and LDPC decoders in collaboration with industry have improved the performance of several generations of smartphones. In collaboration with colleagues at Rice, the distribution of the Rice Wireless open Access Research Platform (WARP) consisting of FPGA and RF components has enabled the broader research community to develop new software defined radio systems. Finally, service to the community is an important responsibility and a way to contribute to future innovation.
My research spans the IEEE Computer, Communications, Signal Processing, and Circuits and System societies. I have had the opportunity to serve in a leadership role in several IEEE conferences and workshops across these societies. I have also served as a former chair of this TC and look forward to chairing the Circuits and Systems for Communications TC in CAS later this year.

Q3. How do you see your research field shaping up and what are the major directions?

These are interesting times with the advances in both hardware and software. A fully interconnected world of smart things and smart cities are exciting new directions that build on advances in VLSI. From new advancements in cloud servers to edge compute nodes to Internet of Things (IoT) sensors there is much for all of us to do. New memory and interconnect technologies will be valuable for improved efficiency in heterogeneous CPU - FPGA - GPU systems for the cloud. New energy harvesting schemes will be critical for ultra-low-power IoT remote sensors. My current research on large scale multiple antenna communication systems (massive MIMO) will allow 5G and beyond wireless systems to provide Gbps performance to large numbers of users. Advances in VLSI signal processing will continue to improve the channel estimation, data detection, and error correction decoding needed to achieve these gains. Due to the scarcity of wireless spectrum, we have been investigating spectrum sharing schemes to enable the future of billions of IoT sensors. Furthermore, as mobile health applications become more widespread, we are investigating energy harvesting strategies for implantable biological sensors and actuators for use in cardiac pacemakers. All of these areas will continue to benefit from new VLSI technologies and architectures on the horizon.

Q4. What advice would you give to junior researchers and graduate students?

It is amazing to witness the current pace of technology. From the 1950’s to today there has been a rapid change in how we communicate and compute that no one could have imagined. VLSI has been a major part of that change from process technology to CAD tools to signal processing algorithms. In many ways, VLSI is a very broad field and requires the integration of knowledge from many specialties. There is a real challenge to keep up to date in new tools and techniques in hardware and software. So, as the field moves into new applications and new technologies, it is important to attend conferences and workshops and to actively read through the IEEE and ACM journals. The IEEE Computer Society TC on VLSI supports many conferences and workshops from the device level to the systems level that are great opportunities for the exchange of new ideas.

Q5. What profession would you be in if you weren’t in this field?

This is an interesting question as the "what if" and the "road not taken" are always moments for reflection. As is the case for many others in our field, math and science have always been a special interest for me. In addition, I have always enjoyed building things, either electronic or mechanical and had spent a lot of time in hobby shops and building various electronic kits from Heathkit back in the 70’s. My father's career was as an architect and my daughter is currently a student in architecture school. So, perhaps if I weren't designing digital systems, I would be designing buildings. In many ways there are many analogies between building organization and structure and art and the functions and material layers in VLSI systems.
Q6. Any final thoughts?

These are exciting times to be at the forefront of new technology! The rapid advances over the last few decades are truly amazing in terms of computing and communications capability. It is always hard to predict the future as new disruptive technologies come up when least expected. I have been fortunate to have been able to contribute to the VLSI revolution over the last thirty years that has led to advances in mobile computing and communications. I am confident that the next thirty years will lead to even further unexpected advances.

Features

Hardware Efficient Second Order Implementation of Sigmoid Function using Distributed Arithmetic
Ravi Kumar and Sanjay Sharma
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Abstract – This letter reports a novel scheme for hardware implementation of the sigmoid function. We propose a piecewise second order approximation that makes use of Distributed Arithmetic (DA) to achieve multiplierless implementation of the second order polynomial using a single 8 word ROM. A dedicated squaring unit has also been used to obtain the square term. A resource efficient implementation for the proposed architecture has been estimated analytically. Actual implementation results and comparison with some existing architectures confirm significant savings in terms of area, gate count and delay. The DA based proposed structure is suitable for cost effective neural emulators and provides the designer ample opportunity to trade-off area and timing parameters as per requirement.

1. Introduction

Implementation of activation functions is of paramount importance for cost effective digital hardware implementation of Artificial Neural Networks (ANNs) which are versatile tools for function approximation, pattern recognition and prediction. Proliferation of Deep Learning (DL) and its universal applicability has redefined the importance of these simple mathematical constructs. DL is the new buzzword in the computational world since it can accurately accomplish the processing of complex data without any pre-processing stage. This phenomenon in the computational science has posed bigger challenges for circuit designers since architectural complexity has now become the most pressing issue. Although recent works have tried to reduce hardware requirements of complex algorithms (e.g. low power health care applications) [1] through innovations at the architectural level, it is pertinent to redesign individual components of ubiquitous computing. A good way to start would be to design an area efficient activation function. Non-linear activation functions like log and tan-sigmoid are used extensively along with Rectified Linear Units (ReLUs) to construct convolutional layers of DL networks [2]. Efficient implementation of nonlinear activation functions with higher accuracy improves the learning and generalization capabilities of neural networks. In this work we propose implementation of the sigmoid activation function described by Eq. 1 as

\[ \text{sig}(u) = \frac{1}{1 + e^{-u}}. \]  (1)
The sigmoid function depicted in Figure 1 satisfies the Riemann integrability condition which implies that it can best be approximated using polynomial functions. However, previous works have reported ingenious methods of piecewise linear approximation [3] and look up table (LUT) based implementations [4-6] apart from piecewise nonlinear (PWNL) schemes [7] and interpolation filter based approximation methods [8]. PWNL approximation guarantees higher precision however at the cost of expensive hardware. Hardware requirements increase with order of approximation polynomial, number of segments to be approximated and length of number representation. To find an optimal trade-off between hardware requirements and function precision, it is necessary to implement PWNL approximation in a hardware efficient manner. In this work, we present a novel method to implement the second order approximated sigmoid function making use of distributed arithmetic (DA). Use of DA yields a multiplier-less architecture without any overhead in terms of delay. Although DA exists as a standard multiply and accumulate (MAC) technique for efficient implementation of bit level architectures, use of DA for nonlinear approximation of sigmoidal function has never been done before to the best of our knowledge. Furthermore, a multiplier-less architecture for nonlinear approximation of sigmoidal activation function is being proposed here for the first time. We start with a second order approximation approach. Similar analysis will hold for higher order approximations.

2. Second order approximation

We follow a 12 bit representation shown as follows.

```
X₃X₂X₁X₀  |  X₋₁X₋₂X₋₃X₋₄X₋₅X₋₆X₋₇X₋₈
```

This employs a fixed point fractional number system with four integer and eight fractional bits. Pervious works [7] have established the optimal choice of the length of representation based on variation of average and maximum error. Based on this we have obtained a maximum error of 0.04 which is indicative of a good precision. We have divided input to sigmoid function into 16 segments. The inputs are uniformly spaced in the domain (-8,8). For a segment, [α, β], if the input \( u \in [α, β] \), using second order approximation the function can be approximated by

\[
\phi(u) = C₀ + C₁ * u + C₂ * u^2
\]  \hspace{1cm} (2)

This operation requires two multipliers and two adders. However, using our technique Eq. (2) can be implemented without multipliers. The technique is described in the following section.

3. The Proposed Technique

Eq. (2) can be written as

\[
\phi(u) = C₀u₀ + C₁ * u^1 + C₂ * u^2
\]  \hspace{1cm} (3)
Eq. (3) can be compared with an inner-product between 2 length-N vectors C and X given by

\[ Y = \sum_{i=0}^{N-1} C_i x_i \]  

(4)

where, \( \{C_i\} \)'s are M-bit constants and \( \{x_i\} \)'s are W-bit 2’s compliment numbers. Eq. (3) and Eq. (4) become identical if \( N=3 \) and \( x_0 = u_0, x_1 = u, \) and \( x_2 = u^2. \) DA efficiently performs vector multiplication given in Eq. (4) as follows:-

Since \( \{C_i\} \)'s are W-bit 2’s complement numbers, they can be expressed as [9]

\[ x_i = -x_{i,w-1} + \sum_{j=1}^{w-1} x_{i,w-1-j} 2^{-j} \]  

(5)

Substituting (5) in (4), we have,

\[ Y = \sum_{i=0}^{N-1} C_i \left( -x_{i,w-1} + \sum_{j=1}^{w-1} x_{i,w-1-j} 2^{-j} \right) \]  

(6)

\[ : Y = -\sum_{i=0}^{N-1} C_i x_{i,w-1} + \sum_{j=1}^{w-1} \left( \sum_{i=0}^{N-1} C_i x_{i,w-1-j} \right) 2^{-j} \]  

(7)

Defining

\[ C_{w-1-j} = \sum_{i=0}^{N-1} C_i x_{i,w-1-j} \quad (j \neq 0) \]  

(8)

and

\[ C_{w-1} = -\sum_{i=0}^{N-1} C_i x_{i,w-1}, \]  

(9)

we have

\[ Y = \sum_{j=0}^{w-1} C_{w-1-j} 2^{-j}. \]  

(10)

Since both C and X are length N vectors, \( x_{i,j} \) has only \( 2^N \) possible values on which \( C_j \) depends. Thus precomputed \( C_j \) value can be stored in a ROM and an input of N bits \( (x_{0,j}, x_{1,j}, \ldots, x_{N-1,j}) \) can be used at an address to retrieve the corresponding \( C_j \) values. One \( Y \) value is produced in \( W \)-clock cycles and intermediate results are accumulated and added to the next accessed content of the ROM using a shift accumulator. This leads to multiplier free realization of vector multiplication. Interestingly, to implement Eq. (3) we require only one 8-word ROM as shown in Table 1.

<table>
<thead>
<tr>
<th>( x_{0,j} )</th>
<th>( x_{1,j} )</th>
<th>( x_{2,j} )</th>
<th>Contents of the ROM</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>( C_2 )</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>( C_1 )</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>( C_{1+2} )</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>( C_0 )</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>( C_{0+2} )</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>( C_{0+1} )</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>( C_{0+1+2} )</td>
</tr>
</tbody>
</table>

An 8-word ROM typically has about 20 gates. Using a multiplication for bit two’s compliment multiplication require logic gates of the order of \( n^2 \). As mentioned above our number system employs a 12 bit representation which means a single multiplier is likely to employ around 144 gates. For a large \( W \), the overhead is primarily in terms of speed since it takes \( W \)-clock cycles to produce one \( Y \) value. Hence in our case vector multiplication require 12 clock cycles. However, if \( j \) consecutive bits are processed in a single clock cycle using \( j \) ROMs, then the input words are processed in \( W/j \)-clock cycles. The same computation can be accomplished in \( \left\lceil \frac{12}{3} \right\rceil = 4 \) clock cycles if 3 ROMs are employed. It can be observed that since \( N \) is a small number, the ROM size is kept small irrespective of fact that we are using 12 bit representation.
Figure 2 depicts the architecture of DA based vector multiplier [9] and Table 2 summarizes unit wise requirement of hardware (in terms of no. of gates) for implementing DA.

![Figure 2: Distributed Arithmetic based vector multiplier](image)

**Table 2: HARDWARE ESTIMATE FOR THE DA UNIT**

<table>
<thead>
<tr>
<th>S. No.</th>
<th>Component</th>
<th>Estimated no. of logic gates</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>$2^i$ word ROM</td>
<td>20</td>
</tr>
<tr>
<td>2.</td>
<td>2:1 MUX</td>
<td>12</td>
</tr>
<tr>
<td>3.</td>
<td>3 bit full adder</td>
<td>27</td>
</tr>
</tbody>
</table>

4. **Multiplier-less Squaring Unit**

The above analysis doesn’t take into account hardware requirements for obtaining square of the input (i.e. $u^2 = x_2$). Squaring operation using multipliers incurs significant hardware overhead specially for higher word length and two’s compliment multiplication. Therefore, we make use of a dedicated squaring unit first reported by Purcell [10]. This circuit makes use of a partial product bit generator which logically AND’s a bit of the n-bit value of weight $2^k$ ($k$ is an integer) with the same bit of weight $2^k$ to provide a partial product bit of weight $2^{2k}$ from a bit of weight $2^k$. The methodology adopted by the inventors is illustrated with the help of Figure 3 and Figure 4. Figure 3 demonstrates multiplication of two 12 bit numbers using conventional binary multiplication. It can be observed that in squaring operation, multiplicand and multiplier bits with same weight generate the same bit after AND operation. In Figure 3 we can observe the partial product bits of weight $2^{2k}$ (in bold) generated from ANDing of bits of weight $2^k$. It can be observed that the bolded bits diagonally divide the array of partial product bits into two. Let us refer to the partial product bits to the upper left and lower right of the bolded bits as “the upper bits” and “the lower bits” respectively.

![Figure 3: Conventional squaring](image)

![Figure 4: Squaring scheme used in this work](image)
Figure 4 demonstrates that same squaring may also be performed by deleting all of the lower bits and by shifting the upper bits 1 bit left. This reduces the number of product bits from $n^2$ (i.e. 144) in the conventional method to $\frac{n(n+1)}{2}$ (i.e. 78) using the method described in Figure 4. In another embodiment of the same methodology the number of product bits can be reduced to 64. The estimated number of logic gates required to implement the polynomial thus stands at 59 (for DA) + 64 (for squaring unit) = 123 which is less than what is required for a single 12 bit multiplier.

5. Results and Analysis

The proposed structure has been implemented with maximum allowable error of 0.04. Verilog hardware description language has been used to write the code and corresponding synthesis has been done by Synopsys Design Compiler using TSMC 0.18 $\mu m$ library. Table 3 presents a comparison of different structures reported in the past with the proposed DA based one. The parameters for comparison are area, gate count, delay, and area delay product. The gate count measure has been defined as the design area normalized with respect to two input NAND gate area. Among other architectures included in the table, the PWL based method proposed by Lin and Wang [4] requires multipliers which results in high area requirement and delay. The other two architectures make use of LUT however, the DA based architecture proposed by us outperforms both LUT and PWL approximation based architectures on all the parameters viz. area, delay and gate count. The greatest saving in terms of area comes from ROM based implementation of vector multiplication. We also have options to improve the delay performance by using $j$ ROMs in parallel so that the vector multiplication could be achieved in $W/j$ clock cycle instead of $W$ clock cycles. Use of an efficient dedicated squaring unit restricts the gate count to less than that required for implementation of a typical $n$ bit multiplier.

<table>
<thead>
<tr>
<th>Structure</th>
<th>Area ($\mu m^2$)</th>
<th>Gate count</th>
<th>Delay (ns)</th>
<th>Area $\times$ Delay ($\mu m^2 \times$ ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Scheme 1[4]</td>
<td>32069.83</td>
<td>3214</td>
<td>903</td>
<td>2.896 $\times$ 10^7</td>
</tr>
<tr>
<td>Scheme 2[5]</td>
<td>9045.94</td>
<td>907</td>
<td>2.15</td>
<td>1.944 $\times$ 10^4</td>
</tr>
<tr>
<td>Scheme 3[6]</td>
<td>3646.83</td>
<td>366</td>
<td>2.31</td>
<td>8.424 $\times$ 10^3</td>
</tr>
<tr>
<td>Proposed</td>
<td>1248.67</td>
<td>126</td>
<td>2.86</td>
<td>3.571 $\times$ 10^3</td>
</tr>
</tbody>
</table>

6. Conclusion

This works defines the implementation of an approximation polynomial as a vector multiplication exercise. This approach has paid dividend since DA proves to be more area efficient for multiplying a small number of vectors. The size of the ROM required is also independent of the word length in the case of DA whereas conventional implementation necessitates use of multipliers resulting in higher (square law) consumption of hardware resources for higher word lengths. Perfect approximation requires representation using higher number of bits and that’s where hardware efficiency of DA is exhibited. Use of a dedicated squaring unit along with DA has resulted in area efficient implementation of sigmoidal function with an impressive area delay product. Work is underway with an aim to further reduce resource consumption in squaring operation.

Reference

Applying Digital Forensic for Hardware Protection: Resolving False Claim of IP Core ownership

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Abstract – This letter reports an intellectual property (IP) core hardware protection approach using digital forensics. The presented Computational Forensic Engineering (CFE) inspired procedure protects ownership of reusable IP cores generated using High Level Synthesis (HLS) through a ‘signature free’ mechanism. The devised a ‘signature free’ (and thus invulnerable to ‘signature tampering’) process incurs 0% hardware overhead compared with digital watermarking.

1. Introduction

Massive competition in electronic industry for maximizing design productivity within given time to market budget has resulted into huge pressure on design engineers. To beat the competition, designers rely heavily on reusable IP cores. Higher level of design abstraction helps in reducing design complexity as well as provides a massive backbone for designing IP cores. Therefore, reusable IP cores generated during higher abstraction level (such as High Level Synthesis (HLS)) have become an integral part of an Integrated Circuit (IC) design flow (fig.1). As mentioned in [1], electronics industry loses approximately 1 trillion USD annually due to piracy and counterfeiting. Therefore, IP protection mechanisms are essential for economic stability of electronics industry.

2. Related Work

There are several threats to an IP core such as Trojan insertion, IP piracy, IP overbuilding, false claim of ownership, etc. The protection methodology with respect to these threats is shown in fig.2. IP metering provides protection against IP piracy and IP overbuilding. Similarly, Logic obfuscation targets protection against IP piracy and Trojan insertion. The only approach that targets protection against false claim of ownership other than customized CFE approach is watermarking. However, watermarking is vulnerable to reverse engineering based attacks such as signature tampering. Further, watermarking approaches may incur hardware overhead due to signature insertion. On the other hand, presented customized CFE based approach is ‘signature free’ and resolves ownership conflicts without incurring any overhead.

3. CFE Approach

In an Ownership conflict scenario, suppose ‘n’ IP vendors (each having their respective HLS tools) are claiming ownership of IP under conflict (IP\textsubscript{C}). The aim of presented CFE approach is to identify with a certain degree of confidence
that IP\textsubscript{C} has been generated using HLS tool of \textsuperscript{i}th vendor where 1 ≤ i ≤ n. As shown in fig.3 adopted from [5], the presented CFE methodology comprises of three steps. In the first step, we study the HLS tool as well as IP of each claimant (IP\textsubscript{vn}) along with IP\textsubscript{C} (given IP core who owner is to be identified) to identify various properties that can distinguish an IP from other IP. These properties are termed as ‘features’ and a set of these features is termed as ‘feature-set’. Once ‘feature-set’ is defined, feature extraction rules are devised for each feature in the ‘feature-set’. These feature extraction rules identify whether a particular feature is present in an IP or not? Subsequently, features extraction process is performed for each of vendor’s IP as well as IP\textsubscript{C}. Finally, ownership is awarded to vendor whose ‘feature-set’ matches 100% with ‘feature-set’ of IP\textsubscript{C} (as per eq. 1) in IP core validation step.

\begin{equation}
\text{Match percent (μ)} = \frac{\text{Number of features matching with IP}_C}{\text{Total number of features in feature set}} \times 100
\end{equation}

Figure 1: Generic IC design flow

Figure 2: Threats and their respective protection methods

Figure 3: Customized CFE approach

4. Case Study on DCT application

In our case study on DCT, we have assumed an ownership conflict between IP vendors of HLS tools [2], [3] and [4]. We have identified three technology independent features that can distinguish between IPs of these tools namely ‘scheduling algorithm’, ‘chaining’ and ‘fault reliability’ [5]. Further, for each of these features in the ‘feature-set’ extraction rules are devised. Figure 4 adopted from [5] shows the devised rules as well as flow graph to identify the type of scheduling algorithm that was utilized to generate an IP. We have limited our case study to only three scheduling algorithms as these are most commonly used scheduling algorithm in HLS tools. The algorithm to extract ‘chaining’ feature is shown in fig.5 (adopted from [5]) where \(CS_{i}(FU_{j})\) and \(CS_{i}'(FU_{j})\) represents starting and ending control step of \(i^{th}\) functional unit (FU). If within the execution time of \(i^{th}\) FU, multiple instances of \(j^{th}\) FU are executed then we say that chaining feature is present in an IP. The final feature we try to extract from IPs, is ‘reliability’ feature. Reliability feature checks for presence of Dual Modular Redundancy (DMR) in top level entity hardware description language (HDL) code of IP core. If DMR is present in an IP, then top level entity datapath HDL code will comprise of a comparator component that has one of its input from original unit (output register signal 1) and another input from duplicate unit (output register signal 2) and comparator’s output signal as final output during port mapping. If such a port mapping is present i.e. port map (output register signal 1, output register signal 2, comparator output signal); in top level entity datapath then it indicates that reliability feature is present in the HDL code of the IP core. The results of our case-study are reported in table 1. The ownership of IP\textsubscript{C} is awarded to IP vendor whose feature-set matches 100% with feature-set of IP\textsubscript{C}. 

\[\text{Ownership is awarded to vendor with feature-set matching of 100%}\]
5. Conclusion

This letter reported a methodology for applying digital forensic process for hardware protection in case of IP ownership conflict. The presented methodology is a signature free approach that incurs no design overhead. The case study on DCT reported that the presented CFE approach is capable of IP protection in case of false claim of ownership.

Acknowledgement

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Reference


Low Power Memristor Based Ring Oscillator: Design and Analysis
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Abstract – There are so many technology options at our disposal to design ring oscillator circuit, but the most efficient technology is to be considered and applied. In this paper a five-stage ring oscillator is proposed based on CMOS technology and memristor based technology. Owing to its significant characteristics, memristor came to the knowledge of researchers and attracted lot of attention worldwide. The Memristor is the fourth element after resistor, inductor, and capacitor. In this paper, a hybrid combination of two kind of technology (CMOS and memristor) is defined and its performance is compared. Memristor based circuit is working on low frequency and performance parameter like power dissipation, noise and delay are reduced as compare to conventional circuit. To design a memristor-based ring oscillator, Pmos transistor is replaced by memristor which leads to reduction of delay and noise. Output level relies on the input state. The drastic reduction of almost 54 percent is seen in power consumption in memristor-based device as compared to conventional device. Noise in memristor-based device has decreased to 0.74 fDB working at 1.2 GHz frequency though in CMOS based device working at same frequency noise produced is 2.84 fDB.

Introduction
The development of Integrated circuit has come as a boon for the world of economics as the size of the devices in electronics is decreased drastically and simultaneously the estimate of power consumption is very economic. The advantage of small chip is that the device can be operated at a very low power supply. In today’s scenario to fetch higher integration, minimum cost with greater speed, the technologies have to be minimised to the required level. The circuit shows anomalous behaviour when the same is operated at the gate length of 90nm for lower voltage supply [1]. The research is intended to know how variations in process, voltage and temperature can affect the circuit behaviour, the references can be made if the root causes in above sentence is to be recognized [2]. This is the result that it has gained important level where the application of wireless communication is to be expected [3]. In constructing a ring oscillator we take odd number of inverters (all connected in series) forming a loop, in order to have different output every time, which automatically results in oscillations. We must provide $2n$ as phase shift with unity voltage gain to extract complete oscillations [4]. The ring oscillator must satisfy Barkhausen criterion for which a $\pi$ phase shift shall be provided with the inversion of DC [5]. Nowadays, world is focusing towards low power circuitry system as our all devices such as mobile tablets, computer systems for which we need to apply it on a large range of frequency, hence the measuring of a frequency is becoming a challenging task.

(a) CMOS Technology Based Ring Oscillator
The ring oscillator was designed using CMOS inverters for five stages. For five stage five inverter cell was cascaded in series [6]-[7]. After connecting the inverters the output of the last inverter is supplied to the input of the initial stage in order to form a ring. In the circuitry, we add noise (VPWL) with different specification for time and voltages to have the oscillations at the output. Without adding the noise to the circuit we can’t expect oscillations at the output. To have the output, ADEL analysis was performed using Cadence Virtuoso tool at 45 nm technology, in that ADEL, transient analysis are done at stop time of 100 ns. The parameters like average power, frequency of oscillations, noise was estimated [7]. All the parameters are compared in between both the ring oscillator with CMOS and with memristor.
In a MOSFET device, the current flowing in channel is modulated by the voltage applied at the gate terminal. In the year 1952, a scientist named Shockley proposed a conventional model for the MOSFET in which he observed three operational modes for the transistor. Equations mentioned below shows the characterization of all the three modes of operation when the channel length of the device increases 10 µm [8].

**Cutoff mode**
Current \( I_D = 0 \), Voltage \( |V_{GS}| \leq |V_T| \)

**Linear mode**
Current \( I_D = \left( \frac{W}{L} \right) \mu C_{ox} \left[ (V_{GS} - V_T)V_{DS} - \frac{1}{2} V_{DS}^2 \right] \),
Voltage \( 0 < |V_{DS}| < |V_{GS} - V_T| \)

**Saturation mode**
Current \( I_D = \frac{1}{2} \left( \frac{W}{L} \right) \mu C_{ox} (V_{GS} - V_T)^2 \),
Voltage \( 0 < |V_{GS} - V_T| < |V_{DS}| \)

Parameters shown in above equations, \( L \) denotes transistor length and \( W \) denotes transistor width, \( \mu \) symbolize as channel mobility carriers.

(b) Memristor

Memristor is named so because it works as a resistor with memory. It builds a relationship between voltage and current across a two terminal device. It behaves as a passive circuit. It is a kind of device which can work on Nanoscale and has ability to substitute the technology named CMOS Physically Uncolonable Functions. The design of memristor consists of two terminals, one terminal is fed with the voltage supply and other is grounded, hence it is perfect for PUF. Memristor is indicated by thick black line in the model [9]. As compared to the CMOS processes, it has greater capacity to produce more randomness and unique in the process variation [10]. The two Scientist namely DaliborBiolek and Zdenek were who created memristor. It is suitable for PUF because of the quality that it can work at low power and area used is very less. Ring oscillator is designed to reduce power consumption and noise in the circuit. Some stipulations are listed below [11]. Figure 2 shows the structure of five-stage ring oscillator replacing a CMOS transistor with a memristor. The value of resistance in ON state = 100Ω, But in OFF state = 16kΩ
(C) Random Number Generator

To provide secret keys, padding, initial vectors, values for masking and nuances in applications for cryptography the True Random Generators are being used [13]. In electronics each and every work is verified on FPGA level. This technique is still a matter of research and discussion when it comes to logic devices and circuit at FPGA. It has emerged as a very essential section of the world. The random number generation must be unique in nature for the user, e.g. we can take an example of a security key. It is not possible to track original key because it has got huge number and thus it provides a secure correlation [14]. Utilizing a huge prime number and raising it to the same strength of the private safe key’s value of the user, a public key can be designed [15].

5. Ring Oscillator: Design and Methodology

(A) Conventional Ring Oscillator

First, the design of a ring oscillator consists of PMOS and NMOS in inverter with single stage. To design the entire ring oscillators Cadence virtuoso tool was used at 45nm of technology. To produce low pass reaction a resistor of value 1KΩ can be used in all the stages. A symbol is created to show the stages on inverters. By combining all the stages a five stage RO was designed. A ring is only possible when the circuitry is having odd numbers of inverters to have oscillations at the output by having delays for each stage and output voltage is measured [16]. The periodic output is dependent upon the resultant voltage. In order to have an oscillation wave the voltage gain at minimum can be estimated for five stages RO. The condition for the oscillations is low frequency gain of 1.236 at each stage at the frequency 0.73 Wo, Where Wo is bandwidth at each stage equal to 3 dB. In frequency response of a system, cutoff frequency is a margin at which power of the system starts to decrease than to pass through. The ratio is one by half; the energy is referred to as 3 dB point. Reduction to 3 dB results around half power [17].

(B) Ring Oscillator with Resistive Load

In this section, single stage inverter design PMOS is replaced by resistive load RD and observe the wave. The configuration of the circuit is known as common source stage with application of resistive load at drain terminal. The variations in voltage of gate-source are transformed into drain current of small signal by an operation performed by this configuration. To create an output voltage it must pass through a resistor. Now, to derive the equation of output voltage large signal for the circuit must be analysed through ally. When the frequency is low, the input provided to the circuit will be high [18]. When input is positive, NMOS of the inverter will go OFF because the output voltage will be equal to VDD. When the input supply voltage will be equal to threshold value, the output voltage will be less and this will turn NMOS on and current will be extracted from the resistor. When the value of VDD is enough, NMOS will be in saturation region.
(C) Memristor Based Ring Oscillator

To replace the resistor of the single stage inverter, five stage RO was designed and performed with the help of memristor to verify the output. The three properties by which a device can be recognized as memristor are:

- In the V-I Plane there is a loop called pinched hysteresis loop.
- As frequency increases area of hysteresis loop will decreases.
- At infinite frequency there is no loop [19].

The different applications of memristor are of high speed memory arrays, adaptive filters, relaxation oscillators and sinusoidal oscillators, and also used in analog and digital circuits, neuromorphic circuits [20]. An advantage of memristor is its compatibility with CMOS as compared to other memory technologies.

6. Performance Parameter

(A) Frequency

The frequency of oscillation for a ring oscillator depends on the delays taking place at the output terminal of the device. By decreasing the stages of a ring oscillator, the operational frequency can be increased. Another method to increase the frequency level is to reduce the total delay of the device [21]. To have constant oscillations, the ring oscillator less than of three stages is not practically feasible. There are some other structural technologies available which help in decreasing the delay and increasing the frequency for a ring oscillator. This structural technology involves coupling and methods of output interpolation.

Frequency of oscillations can be estimated through the following equations [7].

\[ f_o = \frac{1}{2Nt_d} \]

\[ = \frac{I_D}{\eta \cdot N \cdot C_{tot} \cdot V_{DD}} \]

Total capacitance can be calculated by [7]

\[ C_{tot} = \frac{5}{2} C_{OX} \left( L_p W_p + L_n W_n \right) \]

Where,

- \( N \) stands for Number of Delay stages and
- \( t_d \) stands for delay for each stage.

(B) Power Consumption

It goes to explain the average power consumed by the circuit that can be produced by an effective output. For greater performances it is must that efficiency should be high and that can only be achieved by reducing the average power consumed by the circuit.

\[ \text{Power (P)} = V_{DD} \cdot I_{avg} \]

\[ \text{Power (P)} = I_{avg}^2 \cdot R \]

(C) Noise

In the scrutiny of parameter it is basic fact that analog circuit has a property that it is noise free as compare to digital circuit. Noise that occurs randomly in the circuit and disturbs the proper functioning and causing the effect of fluctuation of supply voltage, owing to this phenomenon, the waveform of output of the electronic circuit is also disturbed. Noise restricts the lowest amount of signal level by which circuit could be able to operate with suitable quality.

7. Simulation and Results

Table I analyses all the value of performance parameter which are basically important for a ring oscillator circuit. By the help of this table one can easily compare the difference between two techniques used to design the circuit. Power dissipation has been decreased and also the noise. There is slight increment in leakage current and leakage voltage in memristor based device as compared to CMOS device.
The output waveform of five stage memristor based ring oscillator is shown in the figure 3. The supply voltage of 0.7 V was used at 1.2 GHz of frequency level. The graph is plotted between time (ns) at horizontal axis and voltage (mV) at vertical axis. Transient analysis at stop time 100 ns was done to have the oscillations. The simulation waveform is same for both the technology but the difference is in performance parameter. The temperature used was by default throughout the simulation work.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>CMOS</th>
<th>Memristor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>1.2 GHz</td>
<td>1.2 GHz</td>
</tr>
<tr>
<td>Power consumption</td>
<td>9.199 µW</td>
<td>4.957 µW</td>
</tr>
<tr>
<td>Noise</td>
<td>2.84 fdB</td>
<td>0.74 fdB</td>
</tr>
<tr>
<td>Leakage current</td>
<td>42.10 pA</td>
<td>47.39 pA</td>
</tr>
<tr>
<td>Leakage voltage</td>
<td>140.6 mV</td>
<td>148.8 mV</td>
</tr>
</tbody>
</table>

Figure 3 Output waveform of memristor based Ring Oscillator

In figure 4 the magnitude of frequency, power consumption and noise achieved after the simulation work are shown in the form of bar graph. Graph is used to show the quick glimpse of the values. Graph also shows how the power and noise has decreased at the same frequency level of 1.2GHz, operating at same input voltage supply 0.7 V. With CMOS technology
circuit consumes 9.199 µW whereas with memristor technology circuit consumes 4.957 µW. In conventional circuit noise of 2.84 dB was observed and memristor circuit noise was 0.74 dB.

![Performance Parameter](image)

<table>
<thead>
<tr>
<th>Performance Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
</tr>
<tr>
<td>Memristor</td>
</tr>
</tbody>
</table>

Figure 5 Line Graph to show the difference in parameter

In the figure 5 shown above, line graph is used to show the difference between two technologies. The parameters used in this graph are leakage current and leakage voltage. These two parameters play a very important role in designing of any electronics device. Leakage current in conventional circuit was 42.1 pA and with memristor circuit it was 47.39 pA. In the case of leakage voltage conventional circuit realized 140.6 mV and memristor circuit realized 148.8 mV as leakage voltage.

8. Conclusion

The proposed Ring Oscillator circuits using CMOS and Memristor technology have been simulated successfully on Cadence virtuoso tool in 45 nm. In both circuits a supply voltage of 0.7 V at the frequency of 1.2 GHz was used. Power consumption and noise in memristor circuit is reduced significantly but there is a slight increment in leakage current and leakage voltage as compared to the CMO design. Reduction of power consumption in low power device is a key factor in VLSI environment. CMOS design consumes power as 9.199 µW but in memristor it is reduced to 4.957 µW. Noise in the conventional circuit at 0.7 V is 2.84 dB and in proposed circuit noise is reduced to 0.74 dB. Future research topics could be reduction of leakage current and leakage voltage, as the leakage current and leakage voltage has increased in proposed circuit. So it can be concluded that memristor based ring oscillator has improved performance in power consumption, keeping noise at low frequency range.

References

Highly Optimized SoC Macros for Dongle Type High Performance Singular Value Decomposition Accelerators

Upasna Vishnoi

Abstract – Matrix decomposition accelerators are attractive System on Chip (SoC) components for many applications with a wide range of specifications. This letter elaborates a new family of highly area-efficient and energy-efficient modular matrix decomposition architectures based on the Givens algorithms and Coordinate Rotate Digital Computer (CORDIC) rotations. Accurate algebraic cost models enable for early cost estimation as well as for cross level optimization over architecture, micro-architecture and circuit level using a rich set of parameters. Quantitative results for an exemplary QR Decomposition (QRD) application, implemented in 40-nm CMOS technology are presented.

1. Introduction

Matrix decomposition and matrix factorization techniques are powerful tools of linear algebra and have applications in topics that span sciences. Specifically, QR Decomposition (QRD), Eigen Value Decomposition (EVD) and Singular Value Decomposition (SVD) are applied in sophisticated digital signal processing for image compression, reconstruction and restoration as well as in decoding, space and noise filtering, parameter estimation and source separation in communications, to name just a few. Interesting and very successful research on systolic architectures for real time implementations of matrix decomposition algorithms has been conducted in the 1980’s and 1990’s e.g. [1, 2]. It was found that in comparison to e.g. Householder based approaches, Givens and Jacobi type algorithms feature a high degree of inherent parallelism and can be implemented by mapping the required rotations onto hardware efficient CORDIC operations [3]. However, during those times VLSI-CMOS technology allowed only for implementation of a single CORDIC processor per chip. Today’s very deep submicron CMOS technologies allow for the realization of high throughput, low energy CORDIC macros on a fraction of a square millimeter of silicon area and microwatts of power dissipation [4]. By this, the implementation of high performance matrix decomposition modules to be used as number crunching SoC processor sub-macros has become feasible.

In this work, new architectures and a new methodology for the quantitative optimization of matrix decomposition processor SoC sub-macro implementations for the use in challenging application domains featuring a wide variety of requirements and specifications are elaborated. An attractive target architecture consists of a flexible software controlled Application Specific Instruction Processor (ASIP) executing the matrix decomposition algorithms and being accelerated by a large farm of dedicated CORDIC blocks. The architecture template should allow for the decomposition of real valued matrices as well as complex valued matrices. Floating point capability can be achieved by operating the individual CORDIC blocks in block exponent arithmetic. In order to achieve maximum area and especially energy efficiency, the optimization has to be performed concurrently on all levels of CMOS design, from the algorithmic level down to the physical implementation level. Only by that, the interactions between decisions on the different design levels being imposed by the features of today’s very deep submicron CMOS technologies can be properly considered. A key element of this approach is the elaboration of quite accurate, parameterized algebraic cost models for area, throughput, latency and energy of CORDIC macros [8, 10].

2. QRD Decomposition Accelerators

QR decomposition today for instance is applied in multiple-input/multiple-output (MIMO) channel detection [5, 6, 7]. Suitable CORDIC implementations were investigated and optimized in a 40-nm CMOS technology [4]. Based on the costs of the elementary arithmetic CORDIC sub-functions, a MATLAB based design-space evaluation environment has been elaborated [8]. Key elements to this approach are pre-
characterization of all function slices (adders, shifters etc.) as well as proper interconnect models derived from floorplans. This approach has been successfully validated and optimized by benchmarking against the features of selected exemplary CORDIC implementations [9]. Highly interesting results were achieved especially on the usefulness of applying carry-accelerated (carry select) and redundant (carry save) adder structures.

For the simple most kind of matrix decomposition technique, the QR decomposition, a new “two-way” linear array was derived [10]. The dependency graph depicted in Figure 1 when cut into upper half and lower half and mapped to a 1D signal flow graph as shown in Figure 2 and Figure 3 results as shown in Figure 4; the resulting array is shown in Figure 5 for the simple example of a $n \times n$ matrix with $n=5$. It is composed of $\lfloor n/2 \rfloor$ processing elements and allows for implementation of flexible, micro-code controlled accelerators featuring lowest possible latency as well as high area-efficiency and energy-efficiency. The throughput (and utilization) of that array can be improved by a modification derived from a left-to-right flipping of the dependency graph before mapping. As was shown in [10], there are several possibilities to apply multiplexing in space and/or multiplexing in time to this architecture leading to a high dimensional design space.

Figure 1: QRD dependency graphs for 5x5 matrices optimized for higher throughput rate.

Figure 2: Mapping of the upper half of a 5x5-QRD dependency graph to a 1D signal flow graph.
Based on that as well as on the CORDIC cost models a higher level optimization environment for whole QRD processors have been elaborated [13]. By this, one can account for the strong interactions between QRD architecture, CORDIC micro-architecture and circuit-level, which have not been considered in any publication on QRD architectures so far. The corresponding MATLAB based cost model allows for efficient exploration of the resulting highly complex design space.

Figure 3: Mapping of the lower half of a 5x5-QRD dependency graph to a 1D signal flow graph.

Figure 4: Dependency Graph for a 5x5 QRD and mapping to “two-way” linear arrays ([R] part only).
3. Results

Depending from the specifications a huge design space, featuring up to thousands of possible implementations is available from the QRD-architecture template published in [13]. In order to support design-space exploration the parameterized cost model as well as routines for pruning (e.g. according to maximum latency), Pareto optimization etc. are implemented in a MATLAB-based optimization environment [11]. The execution time for a whole design space exploration (one set of specification parameters) is in the order of a few minutes only. Cost breakdown tables and figures can be generated automatically to get detailed insights to the cost contributions of the individual building blocks in order to identify bottlenecks and to guide optimization. Constraints can be set on the maximum clock frequency e.g. to avoid unreasonably high clock frequencies due to \( a \)-fold Coordinate Rotate Digital Computer multiplexing or on selected clock frequencies being available on a SoC. Arbitrarily high throughput rates can be achieved at almost unchanged ATE complexity and latency by multiplexing parallel QRD blocks [13]. Therefore, especially the area- and energy-optimization for less challenging throughput specifications is a valuable capability of this optimization environment [11]. Finally, it can be applied in early cost estimation to support system conception and design.

In [11], the new QRD-template architecture has been extended for a family of modular architectures allowing also for the decomposition of complex-valued as well as floating-point matrices. Just to show one exemplary result, a QRD macro for 4x4 matrices and 16 bit wordlength implemented in 40-nm CMOS technology can be operated at a clock frequency of 910 MHz, allows for latency as small as 100 ns and a throughput as high as 500 million QRDs per second. Silicon area is 0.0092 mm\(^2\), equivalent gate count is 36.7 k and energy is 5.15 pJ per full QRD (all features are given in worst case corners).
Figure 6 a) : Examples of $AT$ design spaces for complex valued integer full ($[R]$ and $[Q]$) QRD of matrix size $N = 12$

Just to give an idea of the capabilities of the optimization environment exemplary results are in Figure 6 a) which shows an example of $AT$- and $ATE$-design spaces for complex valued integer full ($[R]$ and $[Q]$) QRD of matrix size $N = 12$, iteration count $M = 16$ and wordlength $w = 16$. The whole design space with 1,440 possible implementations is pruned for $ATE \leq 10 \cdot ATE_{\text{min}}$ in Figure 6 b). The execution time for this example is 1 minute 42 seconds, only.
Figure 6 b): Examples of $ATE$-design spaces for complex valued integer full ($\lfloor R \rfloor$ and $\lfloor Q \rfloor$) QRD of matrix size $N=12$

4. Conclusion

A new family of modular two-way linear array QRD architectures based on a new “two-way” linear array is presented. This array is the result of a direct mapping from the dependency graph to a one-dimensional array composed of only $\lfloor n / 2 \rfloor$ processing elements. It allows for a highly area- and energy efficient implementation of QRD accelerators covering a wide application range with real-/complex-valued integer/floating-point matrices.

Generic and parameterized architecture templates have been elaborated and optimized for the QRD array as well as for the PE micro-architecture. An algebraic cost model based on pre-characterization of basic building blocks and proper wiring models allows for efficient and very fast cross-layer exploration of the resulting highly dimensional design space.

5. Outlook: EVD and SVD Accelerators

QRD requires one-sided Givens rotations only. In future, new linear arrays for the implementation of EVD and SVD will be derived by proper mapping of the dependency graphs. This time the challenge on architecture level is that two-sided Jacobi and Jacobi like rotations have to be applied. Initial ideas for achieving highest possible parallelism as well as highest area-efficiency and energy-efficiency are to apply composite rotations as well as customized two-port SRAM modules allowing for row-matrix and column-matrix accesses. Again the MATLAB based cost model will be extended for these architectures to allow for proper design space exploration and early cost estimation in 40-nm and 28-nm CMOS technology.

Finally, the realization of a matrix decomposition accelerator demonstrator in a 28-nm CMOS technology is envisaged, which can be used as a dongle type high performance SVD accelerator to a standard computer.

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Reference
Updates

IEEE VLSI Circuits & Systems Letter

IEEE Computer Society Technical Committee on VLSI
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Opinions: Discussions and book reviews on recent VLSI/nanoelectronic/emerging circuits and systems for nano computing, and “Expert Talks” to include the interviews of eminent experts for their concerns and predictions on cutting-edge technologies.

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ISVLSI: http://www.isvlsi.org
IWLS: http://www.iwls.org
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It’s free, 2-3 Issues/Year
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› Best paper awards
› Timely CFP info

Technical Scope
Various aspects of VLSI design including design of system-level, logic-level, and circuit-level, and semiconductor processes

Join TCVLSI
It’s free to join @ bit.ly/join-tcvlsi

Technical Committee on VLSI (TCVLSI), IEEE-CS
http://www.ieee-tcvlsi.org

IEEE VLSI Circuits and Systems Letter
Volume 4 – Issue 1
Feb 2018
Call for Papers

SPECIAL ISSUE ON:
Hardware-Assisted Techniques for Security and Protection of Consumer Electronics

Editor-in-Chief: Andrew Tyrrell, University of York, UK

The EDA/hardware/VLSI community comprises people from diverse backgrounds (especially hardware and IP cores) leveraged for Consumer Electronics (CE). The electronics design industry is heading for a paradigm shift towards secured, reliable and low cost CE hardware as compared to conventional approaches. With this special section, we aim to present novel solutions for any security/protection problems related to hardware used in CE.

Consumer electronics comprising of high end devices ranging from digital cameras, multi-spectral cameras, smart tablets, and night vision cameras to smart meters, along with information and communication technology could make the emerging concepts of smart cities and Internet of Things (IoT) a reality. In the world of CE, security, privacy, and protection of hardware and its information are equally important. "Hardware-Assisted Security" is defined as the security/protection of hardware/intellectual property (IP) cores of CE devices or information by a hardware/system of CE devices. The term "security" encapsulates a broad theme that covers many aspects including hardware security, protection, privacy, trustworthiness, and IP protection and information security. System security may refer to the security of the system (e.g. a specific CE device) that handles the data or information.

Manuscripts should be scoped within the domain of Hardware-Assisted Security for CE devices and should be original manuscripts prepared in accordance to the normal requirements of IET Computers & Digital Techniques.

Topics covered include:

- Hardware security against Trojans for CE devices
- Forensic engineering based protection of CE hardware
- IP core/hardware security against NBTI attacks on DSP
- Hardware security/IP core protection against reverse engineering attacks for CE devices
- Protection mechanisms of IC/IP buyer
- Protection mechanisms of IC/IP seller
- Energy-efficient digital-rights management hardware for CE
- IP core protection of CE hardware
- Active and passive IP security of CE hardware
- PUF based security and protection methods of CE hardware
- Side channel attack resistant embedded systems, DRM systems

Submit your paper to the manuscript submission and peer review site via the following link:
www.ietdl.org/IET-CDT

Guest Editors:

Anirban Sengupta,
Indian Institute of Technology, India
E: asengupt@iit.ac.in

Garrett S. Rose
University of Tennessee, USA
E: garose@utk.edu

Saraju P. Mohanty
University of North Texas, USA
E: Saraju.Mohanty@unt.edu
IEEE Consumer Electronics Magazine

The IEEE Consumer Electronics Magazine (CEM) is the flagship award-winning magazine of the consumer electronics (CE) society of IEEE. From 2018, the magazine will be published on a bimonthly basis and features a range of topical content on state-of-art consumer electronics systems, services, and devices, and associated technologies.

The CEM won an Apex Grand Award for excellence in writing in 2013. The CEM is the winner in the Regional 2016 STC Technical Communication Awards - Award of Excellence! The CEM is indexed in Clarivate Analytics (formerly IP Science of Thomson Reuters). The impact factor of CE magazine is 1.153.

**Aim and Scope**

- Consumer electronics magazine covers the areas or topics that are related to “consumer electronics”.
- Articles should be broadly scoped – typically review and tutorial articles are well fit for a magazine flavor.
- Technical articles may be suitable but these should be of general interest to an engineering audience and of broader scope than archival technical papers.
- Topics of interest to consumer electronics: Video technology, Audio technology, White goods, Home care products, Mobile communications, Gaming, Air care products, Home medical devices, Fitness devices, Home automation and networking devices, Consumer solar technology, Home theater, Digital imaging, In-vehicle technology, Wireless technology, Cable and satellite technology, Home security, Domestic lighting, Human interface, Artificial intelligence, Home computing, Video Technology, Consumer storage technology. Studies or opinion pieces on the societal impacts of consumer electronics are also welcome.

**Submission Instructions**

Submission should follow IEEE standard template and should consist of the following:

I. A manuscript of maximum 6-page length: A pdf of the complete manuscript layout with figures, tables placed within the text, and

II. Source files: Text should be provided separately from photos and graphics and may be in Word or LaTeX format.
- High resolution original photos and graphics are required for the final submission.
- The graphics may be provided in a PowerPoint slide deck, with one figure/graphic per slide.
- An IEEE copyright form will be required. The manuscripts need to be submitted online at the URL: [http://mc.manuscriptcentral.com/cemag](http://mc.manuscriptcentral.com/cemag)

Have questions on submissions or ideas for special issues, contact EiC at: saraju.mohanty@unt.edu

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- Ezendo Atienza, University of Bedfordshire

CALL FOR PAPERS

Paper Submission Deadline: February 2, 2018
Acceptance Notification: April 2, 2018
Submission of Final Version: May 12, 2018
Special Session Proposal Deadline: February 23, 2018

ISVLSI explores emerging trends and novel ideas and concepts covering a broad range of topics in the area of VLSI: from VLSI circuits, systems and design methods, to system level design and system-on-chip issues, to bringing VLSI methods to new areas and technologies like nano- and molecular devices, hardware security, etc. ISVLSI 2018 highlights a special theme of Internet-of-Things. Future design methodologies are also one of the key topics at the Symposium, as well as new EDA tools to support them. Over three decades the Symposium has been a unique forum promoting multidisciplinary research and new visionary approaches in the area of VLSI, bringing together leading scientists and researchers from academia and industry. Selected high quality papers from ISVLSI 2018 will be considered for two Journal Special Issues: 1) IEEE Transactions on Nanotechnology (impact factor 2.485), and 2) IEEE Consumer Electronics Magazine (impact factor 1.153). The Symposium has established a reputation in bringing together well-known international scientists as invited speakers; the emphasis on high quality will continue at this and future editions of the Symposium.

Contributions are sought in the following areas:

1) Analog and Mixed-Signal Circuits (AMS): Analog/mixed-signal circuits, RF and communication circuits, adaptive circuits, interconnects, VLSI aspects of sensor and sensor network.
2) Computer-Aided Design and Verification (CAD): Hardware/software co-design, logic and behavioral synthesis, simulation and formal verification, physical design, signal integrity, power and thermal analysis, statistical approaches.
3) Digital Circuits and FPGA based Designs (DCF): Digital circuits, chaos/neural/fuzzy-logic circuits, high speed/low-power circuits, energy efficient circuits, near and sub-threshold circuits, memories, FPGA designs, FPGA based systems.
6) Testing, Reliability, and Fault-Tolerance (TRF): Analog/digital/mixed-signal testing, design for testability and reliability, online testing techniques, static and dynamic defect- and fault-recoverability, and variation aware design.

The Symposium Program will include contributed papers and speakers invited by the Program Committee as well as a poster session. The keynotes, special sessions and Student Research Forum are planned as well. Authors are invited to submit full-length, original, unpublished papers. To enable blind review, the author list should be omitted from the main document. Initial submissions to the conference are limited to six pages in PDF format.

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Membership Fee: $20
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Benefits Include:
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2) Discount in conference registration
3) Networking opportunity with global peers

Your Professional Experience
(circle your choices below)

I have graduated from a three-to-five-year academic program with a university-level degree.
This academic institution or program is accredited in the country where the institution is located.
Yes No Do not Know

I have _______ years of professional experience in teaching, creating, developing, practicing, or managing within the following field:

- Engineering
- Computer Sciences and Information Technologies
- Physical Sciences
- Biological and Medical Sciences
- Mathematics
- Technical Communications, Education, Management, Law and Policy
- Other (please specify) _____________________________

Are you or were you ever a member of the IEEE? Yes No
If Yes, provide, if known:

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Grade _____________________________
Year of Expiration if no longer a member _________

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- □ IEEE Member, joining CE Society

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Signature

For Office Use Below

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IEEE Recruiter's Member Number _____________________________

Online at: https://cesoc.ieee.org/membership.html
iNIS 2017 IEEE TCVLSI Best paper awards:

Subhendu Kumar Sahoo, P. K. Meher, "Lookup Table-Based Low-Power Implementation of Multi-Channel Filters for Software Defined Radio"

Shrestha Bansal, Hemanta Kumar Mondal, Sri Harsha Gade, Sujay Deb, "Energy Efficient NoC Router for High Throughput Applications in Many-core GPUs"

Anirban Sengupta, Dipanjan Roy, "Mathematical Validation of 2D HWT based Lossless Image Compression for CE applications"

iNIS 2017 IEEE TCVLSI Travel Awards:

1. Saranyu Chattopadhyay, IIT Kharagpur
2. Naga Sasikanth Mannem, IIT Kharagpur
3. Pritam Bhattacharjee, NIT Arunachal Pradesh

SLIP 2017
For travel grant, the information of both students is as follows:

Leo Filippini
Drexel University
lf458@drexel.edu

Peishan Tu
Chinese University of Hong Kong
tpeisharon@gmail.com

For the best paper award, the contact window of the awardee is as follows:

Timing Driven Routing Tree Construction
Pershan Tu, Wing-Kai Chow, and Evangeline Young

Chinese University of Hong Kong
tpeisharon@gmail.com
The International Symposium on Asynchronous Circuits and Systems (ASYNC) is the premier forum for researchers to present their latest findings in asynchronous design. Authors are invited to submit papers on any aspect of asynchronous design, ranging from design, synthesis, and test to asynchronous applications.

Topics of interest include:
-- Asynchronous pipelines, architectures, CPUs, and memories
-- Asynchronous ultra-low power systems, energy harvesting, and mixed-signal/analogue
-- Asynchrony in emerging technologies, including bio, neural, nano, and quantum computing
-- CAD tools for asynchronous design, synthesis, analysis, and optimization
-- Formal methods for verification and performance/power analysis
-- Test, security, fault tolerance, and radiation hard design
-- Asynchronous variability-tolerant design, resilient design, and design for manufacturing
-- Asynchronous design for neural networks and machine learning applications
-- Circuit designs, case studies, comparisons, and applications
-- Mixed-timed circuits, clock domain crossing, GALS systems, Network-on-Chip, and multi-chip interconnects
-- Hardware implementations of asynchronous models and algorithms, asynchronous techniques in clocked designs, and elastic and latency-tolerant synchronous design

Paper Format and Submission:
Submissions for regular and special topics must report original scientific work, in 6-8 pages IEEE double-column conference format (single-spaced, 10pt or larger font size), with author information concealed. Accepted papers will be published in the IEEE digital library and IEEEXplore symposium proceedings.

"Fresh Ideas" / Student Posters
We solicit 1-2 page submissions that present "fresh ideas" in asynchronous design, not yet ready for publication. These will go through a separate light-weight review process. Accepted submissions will be assembled in a binder and handed out at the workshop. We also invite students to present a poster on their research, co-authored with their advisor, and to submit a 1 page abstract that will receive a light-weight review.

Industrial Papers / Tools & Demos
ASYNC 2018 will include papers and tutorials from industry on the state-of-the-art application of asynchronous designs to both existing and emerging technologies. The topics are specifically targeted at industry and include:
-- Synchronizers and clock domain crossing techniques
-- Techniques for combining asynchronous and clocked designs
-- CAD tools for integrating asynchronous circuits with clocked designs
-- Circuit designs, case studies, comparisons, and applications

We solicit 1-2 page submissions for the workshop, IEEE double-column conference format. These papers will go through a separate light-weight review process. Accepted papers will be published in the IEEE digital library IEEEXplore and symposium proceedings. We also solicit tools and demos for presentation at the conference.

Important Dates

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<th>Category</th>
<th>Regular Papers</th>
<th>Other categories</th>
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<td>Abstract registration deadline</td>
<td>Nov 26, 2017</td>
<td>Feb 14, 2018</td>
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<tr>
<td>Paper submission deadline</td>
<td>Dec 3, 2017 (abstracts only)</td>
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<tr>
<td>Notification of acceptance</td>
<td>Feb 7, 2018</td>
<td>Feb 28, 2018</td>
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<tr>
<td>Publication-ready final version due</td>
<td>Mar 10, 2018</td>
<td>Mar 10, 2018</td>
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</table>
The IEEE Russia (Northwest) Section and the IEEE Russia (Northwest) Section BT/CE/COM Joint Chapter prolong submission of technical papers for oral and poster presentations at the 22nd annual conference, IEEE ISCT International Symposium on Consumer Technologies (former International Symposium on Consumer Electronics) that takes place in St-Petersburg, Russia on 11th - 12th May 2018. Now the important dates of ICCT are the following:

Submission Deadline: January 29, 2018
Acceptance Notification: February 19, 2018
Submission of Final Version: March 05, 2018

The theme of ISCT 2018 is “Consumer Technologies in 10 years”.

Paper contributions are sought in but are not limited to following areas:

- Internet of Things and Internet of Everywhere (IoT)
- Consumer Healthcare Systems (CHS)
- Energy Management of CE Hardware and Software Systems (EMC)
- Application-Specific CE for Smart Cities (SMC)
- Artificial Intelligence in Consumer Technologies (AIC)
- Consumer Technologies Quality and Testing (CTQ)
- Telecom and Network Technologies (TNT)
- AV Systems, Image and Video, Cameras and Acquisition (AVS)
- CE Sensors and MEMS (CSM)
- Smartphone and Mobile Device Technologies (MDT)
- Entertainment, Gaming, Virtual and Augmented Reality (EGV)
- TV, RF and Wireless Technologies (TRW)
- Education in Consumer Technologies Area (EDU)
- Other Technologies Related with CE (MIS)

Authors are invited to submit original, unpublished manuscripts of 2- to 6-page length at https://edas.info/newPaper.php?c=24269 (the link can be also accessed from the conference website). Previously published papers or papers under review for other conferences/journals should not be submitted for consideration. Authors may prepare original work of maximum 6 pages with a 200-word abstract using double-column IEEE conference-format template: https://www.ieee.org/conferences_events/conferences/publishing/templates.html

All accepted papers (including regular papers and special session papers) will be published in the ISCT 2018 Proceedings and submitted to IEEE Xplore. Instructions for authors and document templates are available on the conference website.
Registration information and prices as well as patronage opportunities are also published on the conference website https://www.isct2018.ru. Prices start with 100 Euro.

Sincerely yours,
Dr. Dmitry Vavilov, ISCT 2018 General Chair
Dmitry.Vavilov@t-systems.com

<table>
<thead>
<tr>
<th>Title</th>
<th>Program Guidelines</th>
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<td>Computational and Data-Enabled Science and Engineering (CDS&amp;E)</td>
<td></td>
<td>Full Proposal:November 15, 2018</td>
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<tr>
<td>CISE Research Infrastructure (CRI)</td>
<td>17-581</td>
<td>Preliminary Proposal:November 7, 2018</td>
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| Computational and Data-Enabled Science and Engineering (CDS&E) | | Full Proposal:November 1, 2018  
Full Proposal:October 31, 2018 |
| Graduate Research Fellowship Program (GRFP) | 16-588 | Full Proposal:October 26, 2018  
Full Proposal:October 25, 2018  
Full Proposal:October 23, 2018  
Full Proposal:October 22, 2018 |
<p>| Industry-University Cooperative Research Centers Program (IUCRC) | 17-516 | Preliminary Proposal:October 17, 2018 |
| Computational and Data-Enabled Science and Engineering (CDS&amp;E) | | Full Proposal:October 15, 2018 |
| Historically Black Colleges and Universities Undergraduate Program (HBCU-UP) | 18-522 | Full Proposal:October 2, 2018 |
| Computational and Data-Enabled Science and Engineering (CDS&amp;E) | | Full Proposal:October 1, 2018 |
| Innovations in Graduate Education (IGE) Program | 17-585 | Full Proposal:September 27, 2018 |</p>
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<td>International Research Experiences for Students (IRES)</td>
<td>18-505</td>
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<td>Computational and Data-Enabled Science and Engineering (CDS&amp;E)</td>
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<td>Full Proposal:September 17, 2018</td>
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<td>International Research Experiences for Students (IRES)</td>
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<tr>
<td>Computational and Data-Enabled Science and Engineering (CDS&amp;E)</td>
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<td>Historically Black Colleges and Universities Undergraduate Program (HBCU-UP)</td>
<td>18-522</td>
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<td>Preliminary Proposal:April 25, 2018</td>
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## Funding Opportunities

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<td>Industry-University Cooperative Research Centers Program (IUCRC)</td>
<td>17-516</td>
<td>Preliminary Proposal:April 18, 2018</td>
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<tr>
<td>Innovation Corps (I-Corps TM) - National Innovation Network Nodes Program (I-Corps™ Nodes)</td>
<td>17-533</td>
<td>Full Proposal:March 13, 2018</td>
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<tr>
<td>Historically Black Colleges and Universities Undergraduate Program (HBCU-UP)</td>
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<td>Full Proposal:March 1, 2018</td>
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<td>Smart and Connected Communities (S&amp;CC)</td>
<td>18-520</td>
<td>Full Proposal:February 28, 2018</td>
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<td>EMERGING FRONTIERS IN RESEARCH AND INNOVATION 2018</td>
<td>17-578</td>
<td>Full Proposal:February 23, 2018</td>
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<td>National Robotics Initiative 2.0: Ubiquitous Collaborative Robots (NRI-2.0)</td>
<td>18-518</td>
<td>Full Proposal:February 20, 2018</td>
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<tr>
<td>Training-based Workforce Development for Advanced Cyberinfrastructure (CyberTraining)</td>
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<td>Full Proposal:February 14, 2018</td>
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<tr>
<td>International Research Experiences for Students (IRES)</td>
<td>18-505</td>
<td>Full Proposal:February 13, 2018</td>
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<tr>
<td>Innovation Corps (I-Corps TM) - National Innovation Network Nodes Program (I-Corps™ Nodes)</td>
<td>17-533</td>
<td>Letter of Intent:February 8, 2018</td>
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<tr>
<td>Innovation Corps- National Innovation Network Sites Program (I-Corps Sites)</td>
<td>16-547</td>
<td>Full Proposal:February 8, 2018</td>
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<tr>
<td>International Research Experiences for Students (IRES)</td>
<td>18-505</td>
<td>Full Proposal:February 6, 2018</td>
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# Funding Opportunities

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<tr>
<th>Title</th>
<th>Program Guidelines</th>
<th>Due Dates</th>
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<tr>
<td>National Science Foundation Research Traineeship (NRT) Program</td>
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<td>Full Proposal:February 6, 2018</td>
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<tr>
<td>Major Research Instrumentation Program: (MRI)</td>
<td>18-513</td>
<td>Full Proposal:February 5, 2018</td>
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<td>Partnerships for Innovation (PFI)</td>
<td>18-511</td>
<td>Full Proposal:February 1, 2018</td>
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<tr>
<td>Campus Cyberinfrastructure (CC*)</td>
<td>18-508</td>
<td>Full Proposal:January 30, 2018</td>
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<tr>
<td>International Research Experiences for Students (IRES)</td>
<td>18-505</td>
<td>Full Proposal:January 30, 2018</td>
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<td>Smart and Connected Communities (S&amp;CC)</td>
<td>18-520</td>
<td>Letter of Intent:January 30, 2018</td>
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<tr>
<td>EPSCoR Research Infrastructure Improvement Program: Track-2 Focused</td>
<td>18-502</td>
<td>Full Proposal:January 26, 2018</td>
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<tr>
<td>Spectrogram: Energy Efficiency, and Security (SpecEES): Enabling</td>
<td>17-601</td>
<td>Full Proposal:January 18, 2018</td>
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<tr>
<td>ADVANCE: Increasing the Participation and Advancement of Women in</td>
<td>16-594</td>
<td>Full Proposal:January 17, 2018</td>
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<td>Academic Science and Engineering Careers</td>
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<tr>
<td>Historically Black Colleges and Universities Undergraduate Program</td>
<td>18-522</td>
<td>Letter of Intent:January 16, 2018</td>
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<td>(HBCU-UP)</td>
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<td>NSF/Intel Partnership on Foundational Microarchitecture Research</td>
<td>17-597</td>
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<td>CISE Research Infrastructure (CRI)</td>
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<td>Collaborative Research in Computational Neuroscience (CRCNS)</td>
<td>18-501</td>
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<tr>
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<td>Cyberinfrastructure for Emerging Science and Engineering Research (CESER)</td>
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<td>Full Proposal:Accepted Anytime</td>
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Funding Opportunities

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<tr>
<td>Innovation Corps - National Innovation Network Teams Program (I-Corps™ Teams)</td>
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<td>17-594</td>
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Announcements for Academic, Postdoctoral and PhD Positions

| AcademicKeys | http://www.academickeys.com/ |
| HigherEdJobs | https://www.higheredjobs.com/ |
| IEEE Job Site | http://jobs.ieee.org/ |
| IEEE Computer Society | https://www.computer.org/web/jobs |
| Computing Job Announcements – CRA | https://cra.org/ads/ |

Call for Nominations of Awards – IEEE-CS TCVLSI

IEEE-CS TCVLSI Technical Excellence Award
The IEEE-CS TCVLSI Technical Excellence Award recognizes significant and sustained contributions of professionals to the VLSI community through the IEEE Technical Committee on VLSI (TCVLSI). The award is based on the impact of high-quality research (evident through publications within premier IEEE periodicals) made by the awardee in 1) emerging topics during the past five (5) years, and 2) overall research contributions in at least the last ten (10) years. Additionally, the candidate must show evidence of significant contributions made to the growth and sustainability of IEEE Technical Committee on VLSI. The candidate must be an IEEE Senior Member or Fellow (or equivalent in other Professional Societies such as ACM or IET) to be considered. The award consists of a plaque and a citation.

IEEE-CS TCVLSI Distinguished Leadership Award
The IEEE-CS TCVLSI Distinguished Leadership Award recognizes significant and outstanding contributions to the TCVLSI community in a leadership position. The award is based on the impact of contributions/services rendered for the growth of TCVLSI across the globe. The candidate must be in a leadership position within TCVLSI, and have demonstrated excellence in shaping the TCVLSI in terms of research or community growth for a period of at least four (4) years. The candidate must be an IEEE Senior Member or Fellow (or equivalent in other Professional Societies such as ACM or IET) to be considered, and must have an outstanding research profile for a period of at least the last twelve (12) years. The award consists of a plaque and a citation.

IEEE-CS TCVLSI Distinguished Research Award
The IEEE-CS TCVLSI Distinguished Research Award recognizes significant and outstanding research contributions to the VLSI community through a leadership position. The award is based on the impact of research contributions made to the VLSI community. The candidate must be in a leadership position and have demonstrated research excellence for a period of at least fifteen (15) years. The candidate must be an IEEE Senior Member or Fellow (or equivalent in other Professional Societies like ACM, IET) to be considered and must be an active member of TCVLSI community. The award consists of a plaque and a citation.

IEEE-CS TCVLSI Mid-Career Research Achievement Award
The IEEE-CS TCVLSI Mid-Career Research Achievement Award recognizes contributions of professionals in terms of high quality research in the field of VLSI (especially emerging areas that is provides a paradigm shift). Eligible candidates must have evidence of strong publications in premier IEEE periodicals related to VLSI (or equivalent area) consistently for a period of at least four (4) years, as well as high quality overall research for a period of at least ten (10) years, all obtained through independently led research. Eligible candidate must be an active member of TCVLSI community. The candidate must be an IEEE Senior Member or Fellow (or equivalent in other Professional Societies such as ACM or IET) to be considered. The award consists of a plaque and a citation.

IEEE-CS TCVLSI Outstanding Editor Award
The IEEE-CS TCVLSI Outstanding Editor Award recognizes sustained contributions of a IEEE VCAL Editorial Board member made for a period of at least two (2) years. The candidate must demonstrate evidence of contribution made that led to the growth of VCAL and must be an active member of TCVLSI community.

Deadline for notification of successful award recipient: March 15, 2018.
The “Call for Nominations” is announced in TCVLSI website and VCAL Feb issue.

Notes:
(a) All the above dates are tentative and may be subjected to minor change in case of timing conflicts.
(b) If in any year, no application is deemed suitable for the above awards, the committee will be empowered to not award anyone for a specific year(s). The decision of award committee is final on the award matters.

Nominations should be accompanied by ‘CV’ and ‘1-page Statement of Contribution’ and email to cavallar@rice.edu for evaluation by the awards committee (please see details on award committee on TCVLSI website). Please include the name of the award category in the subject line.

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Post-Conference Report
of the TCVLSI Sponsored Conferences in 2017

In 2017, TCVLSI sponsored 9 conferences and technically co-sponsored 2 conferences.

Sponsored Conferences:
ARITH 2017 organized 7 technique sessions, i.e., (1) Multiprecision arithmetic, (2) Arithmetic operators, (3) Floating-point error analysis, (4) Hardware for fast and reproducible arithmetic, (5) Arithmetic in FPGAs, (6) Cryptography and (7) Miscellaneous topics in computer arithmetic. It also organized 2 special sessions, i.e., (1) Realizing efficient matrix computations and (2) Arithmetic in DSP. ARITH 2017 host 2 keynote talks, i.e., (1) “The rise of multiprecision arithmetic” given by N. Higham from Manchester University and (2) “Large scale numerical simulations of the climate” given by J-C. Rioual from Met Office at UK. The general chair of ARITH 2017 was Neil Burgess from ARM in UK and the program chairs were Javier Bruguera from ARM in USA and Florent de Dinechin from INSA Lyon in France.

2. IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), July 10-12 2017, Seattle, USA:
ASAP 2017 organized 7 technique sessions, i.e., (1) Machine learning, (2) Security, (3) Image processing, (4) Memory/Storage, (5) High performance computing, (6) Digital signal processing and (7) Control systems and parallel programming languages. It also organized a panel discussion for “Industry and academic collaboration” and 2 keynote talks, i.e., (1) “Performance is overrated or: how I stopped worrying and learned to love slow hardware” given by Tim Sherwood from UC Santa Barbara and (2) “Accelerated computing on AWS: applications for GPUs and FPGAs” given by David Pellerin from Amazon Web Services. The general chair of ASAP 2017 was Ken Eguro from Microsoft Research and the program chair is Ryan Kastner from the University of California, San Diego.

ASYNC 2017 organized 7 technique sessions, i.e., (1) Intra-chip communication, (2) Metastability and arbitration, (3) Asynchronous interfaces and NoCs, (4) Modelling and design automation, (5) Delay lines and bundled data design, (6) Theory, analysis, and test and (7) Application of asynchronous designs. It invited 3 keynote speakers, i.e., John Redmond from Broadcom, Keith Bowman from Qualcomm and Ken Yun from UCSD. The submission deadline of the regular track full papers was extended from December 16, 2016 to December 2, 2016. The general chairs of ASYNC 2017 were Matheus T. Moreira from USA and Peter A. Beerel from USA. The program chairs were Edith Beigné from France and Ken Stevens from USA.

4. IEEE International Symposium on Nanoelectronic and Information Systems (iNIS), December 18-20, 2017, Bhopal, India (To go with the technology trend this meeting will be renamed to IEEE International Symposium on Smart Electronic Systems (iSES), http://www.ieee-ises.org, to be at Hyderabad, India, during 17-19 December 2018):

It also organized 7 special sessions, i.e., (1) Emerging nanoscale transistors for biosensing and IoT applications, (2) Circuit design in rebooting computing, (3) Applications of big data analytics and IoT for tomorrow’s smart city, (4) MOS current mode logic: an alternative for high speed signaling, (5) Gated clock distribution for silicon chips, (6) Networks-on-Chip architecture and (7) IoT and smart cities, and host 5 keynote talks, i.e., (1) “ThirdEye: visual assist for grocery shopping” given by Vijaykrishnan Narayanan from Pennsylvania State University, PA , USA, (2) “Challenges of converging nanoelectronics and nanotechnology for internet of things” given by Durgamadhab
(Durga) Mishra from New Jersey Institute of Technology Newark, NJ, USA, (3) “QUADSEAL: a hardware countermeasure against side channel attacks on AES” given by Sri Parameswaran from the University of New South Wales, Australia, (4) “Considerations for designing secure and efficient nano electronic computer architectures” given by Garrett S. Rose from the University of Tennessee, Knoxville, TN 37996-2250 USA and (5) “Reduced dimension-based emerging novel switching transistors and interconnects for post-CMOS electronics” given by Ashok Srivastava from Louisiana State University, Baton Rouge, USA.

The submission deadline of iNIS 2017 was extended from July 28, 2017 to August 15, 2017. The general chairs of iNIS 2017 were Dhruva Ghai from Oriental University, India, Xin Li from Duke University, USA and Prasun Ghosal from IIEST, India. The program chairs were Sudeep Pasricha from Colorado State University, USA, Anirban Sengupta from IIT Indore, India and Jawar Singh from IIITDM, India.

5. IEEE Computer Society Annual Symposium on VLSI (ISVLSI), July 3-5, 2017, Bochum, Germany:
ISVLSI 2017 organized 6 technique sessions, i.e., (1) Digital circuits and FPGA based designs, (2) Emerging and post-CMOS technologies, (3) System design and security, (4) Testing, reliability, and fault-tolerance, (5) Computer-aided design and verification and (6) Analog and mixed-signal circuits, and 5 special sessions, i.e, (1) Post CMOS computing: emerging technologies and design issues, (2) Emerging computing paradigms for energy-efficient and secure IoT devices, (3) Adaptive circuits and systems for machine intelligence: the role of adaptive circuits and systems in emerging intelligent systems and networks, (4) Emerging and secured applications of IoT, (5) Innovation in memory technologies and their applications.

ISVLSI 2017 host a distinguished lecture “Pushing the limits of technology, circuit and applications for sub-nm low power design” given by Rajiv Joshi from T. J. Watson research center, IBM and 3 keynote talks, i.e., (1) “Electronic circuit design for the smart world era” given by Georges Gielen from University of Leuven, (2) “History and future of megatrends in EDA industry” given by Mr Jens C. Werner, the Vice President of Cadence and (3) “What about increasing the functionality of devices rather than scaling them?” given by Pierre-Emmanuel Gaillardon from University of Utah. The general chairs of ISVLSI 2017 were Michael Hubner from Ruhr-University of Bochum, Germany and Ricardo Reis from UFRGS, Brazil. The program chairs were Mircea Stan from University of Virginia, USA and Nikos Voros from Technological Educational Institute of Western Greece, Greece.

6. IEEE International Workshop on Logic & Synthesis (IWLS), June 17-18, 2017, Austin, TX:
IWLS 2017 organized 5 technique sessions, i.e., (1) Let’s get warmed up: logic synthesis, (2) More synthesis: engineering change order, synthetic biology, stochastic computing, (3) Designer’s best friends: XAIGs, BDDs, and MAJ, (4) Is everything correct?: verification and (5) Last, not least: high-level, compilation, and mapping. It also organized 1 special sessions for “Advances in formal verification” and host 2 keynote talks, i.e., “DA perspectives and futures: an update” given by Andrew B. Kahng from UC San Diego and “Machine learning in formal verification” given by Manish Pandey from Synopsys. The general chair of IWLS 2017 was Jie-Hong Roland Jiang from National Taiwan University, Taiwan. The program chairs were Rolf Drechsler from the University of Bremen/DFKI GmbH, Germany and Robert Wille from Johannes Kepler University Linz, Austria.

7. IEEE International Conference on Microelectronic Systems Education (MSE) May 11-12, 2017, Banff, Canada:
MSE 2017 organized 2 technical sessions about (1) Pedagogical innovations using a wide range of technologies (e.g., nanometer-scale integrated circuits, low-power design, nanotechnology, etc.), (2) Educational techniques (e.g., novel curricula and laboratories, assessment methods, etc.), (3) Industry and academic collaborative programs and teaching
and (4) preparing students for industry, entrepreneurship, academics, and/or research. It host 3 keynote talks, i.e., (1) “Internet-of-Medical-Things” given by Niraj K. Jha from Princeton University, (2) “FPGAs in the datacenter - combining the worlds of hardware and software development” given by Andrew Putnam from Microsoft and (3) “Green computing: new challenges and opportunities” given by Alex Jones from University of Pittsburgh. The general chair of MSE 2017 was Ozcan Ozturk from Bilkent University and the program chair was Tina Hudson from Rose-Hulman Institute of Technology.

8. **ACM/IEEE System Level Interconnect Prediction (SLIP), June 17, 2017, Austin, USA:**
SLIP 2017 organized 3 technique sessions, i.e., (1) Routing, (2) DFM and routing and (3) Clocking. It host 1 keynote talk about “Frontiers of timing” given by Ulf Schlichtmann from Technical University of Munich and 1 panel on “Neuromorphic computing and deep learning”. The general chair of SLIP 2017 was Tsung-Yi Ho from National Tsing Hua University, Taiwan and the program chairs were Shiyan Hu from National Tsing Hua University, Taiwan and Mustafa Badaroglu from Qualcomm Inc., USA.

9. **IEEE International Workshop of Electronics, Control, Measurement, Signals and their application to Mechatronics (ECMSM), May 24-26, 2017, Orona IDeO, Orona:**
ECMSM 2017 organized 8 technique sessions, i.e., (1) Images processing, (2) Signal acquisition and processing, (3) Fault detection and diagnosis in mechatronic, (4) Sensors and measurement, (5) Electrical drives and control, (6) Robotics and autonomous systems, (7) Actuation, (8) Analog/Hybrid design and (9) Networking and operating systems. It host 3 keynote talks, i.e., (1) “Easy configuration of collaborative robots” given by Ole Madsen from Aalborg University, Denmark, (2) “MANTIS project: cyber physical system based proactive collaborative maintenance” given by Urko Zurutuza from Mondragon University, Spain and (3) “Challenges and solutions for Internet of things in the industry” given by Josu Bilbao from IK4-Ikerlan Research Center, Spain. The general chair of ECMSM 2017 was Juan Carlos Mugarza from Mondragon University and the program chair was Nestor Arana-Areolaleiba also from Mondragon University.

**Technically Co-Sponsored Conferences:**

1. **International Conference on Application of Concurrency to System Design (ACSD), June 28-30, 2017 Zaragoza, Spain:**
ACSD 2017 organized 7 technique sessions, i.e., (1) Verification of timed systems, (2) Compositional verification, (3) Asynchronous systems, (4) Circuit analysis, (5) Models of concurrency, (6) Scheduling of concurrent systems and (7) Shared memory concurrency. It host a Distinguished Carl Adam Petri Lecture on “Promises and challenges of reactive modeling: a personal perspective” given by Thomas A. Henzinger from Institute of Science and Technology, Austria and 7 invited talks, i.e., (1) “The alignment of formal, structured and unstructured process descriptions” given by Josep Carmona from Universitat Politècnica de Catalunya, Spain, (2) “Complexity made simple at a small price” given by Christos G. Cassandras from Boston University, USA, (3) “Resource equivalences in Petri nets” given by Irina Lomazova from National Research University Higher School of Economics, Moscow, Russia, (4) “Property-preserving generation of tailored benchmark Petri nets” given by Jaco van de Pol from University of Twente, The Netherlands, (5) “Modelling & Mining event-based concurrent declarative processes as dynamic condition response graphs” given by Thomas Hildebrandt from University of Copenhagen, Denmark, (6) “Model-driven development of performance sensitive cloud native streaming applications” given by José Ángel Bañares from University of Zaragoza, Spain and (7) “Verification of reconfigurable Petri nets” given by Julia Padberg from Hamburg University of Applied Sciences, Germany. The program committee chairs of ACSD 2017 were Alex Legay from France and Klaus Schneider from TU Kaiserslautern, Germany.
2. **International Conference on VLSI Design (VLSID), January 7-11, 2017, Hyderabad, India:**


It host 14 tutorials, i.e., (1) “22fdx FDSOI application towards IOT for smart devices” given by Mahbub Rashed from GlobalFoundries, (2) “Memory is everywhere” given by John Barth and Bipin Malhan from INVECAS, India, (3) “Thermal aware testing of VLSI circuits and systems” given by Santanu Chattopadhyay and Rajit Karmakar from IIT-Kharagpur, India, (4) “Evolved supply set based UPF methodology” given by Aman Jain from Seagate Technology India, (5) “The world beyond DRC: Design for Manufacturing (DFM) - impact on yield & reliability for advanced technology nodes and their elucidations” given by Yadav Preet from NXP Semiconductors India, (6) “High level modeling of digital circuits” given by V. Kamakoti from IIT Madras, India, (7) “Designing with xilinx SDSoC” given Chandra Sekar and Hemasunder from Xilinx, India, (8) “Communication infrastructure for future exascale processors” given by Sujay Deb, Sri Harsha Gade and Hemanta Kumar Mondal from IIT-Delhi India, (9) “Devices and circuits to address the challenges in IOT” given by Ayan Datta, M. Ramakrishna, Sarvesh Verma and Saikrishna Joganapally from Intel Technologies India, (10) “Memristors: technology, circuit models and applications” given by Kamalika Datta and Indranil Sengupta from National Institute of Technology, Meghalaya, (11) “Design of energy and area efficient circuits using spin devices in combination with CMOS” given by Mohammad Hasan from Aligarh Muslim University, Aligrah, (12) “Design, simulation, fabrication and testing of microwave CMOS distributed oscillators, amplifiers, noise cancelling LNA with temperature performances and finally design of 60 GHz 5G receiver for mobile communication” given by Kalyan Bhattacharyya from Amrita University, Coimbatore India, (13) “Pushing the envelope on ultra-high speed SerDes interfaces” given Srinivas Murthy and Nagarajan Viswanathan by from TI, India, and (14) “Privacy assurance in the IoT world” given by Paramesh Ramanathan from University of Wisconsin, Madison USA.

The **general chair** of VLSID 2017 was Dasaradha R Gude (GD) from INVECAS and the **technique program chairs** were Vijay Raghunathan from Purdue University, USA and Kanishka Lahiri from AMD.
Call for Contributions

The VLSI Circuits and Systems Letter aims to provide timely updates on technologies, educations and opportunities related to VLSI circuits and systems for TCVLSI members. The letter will be published quarterly a year (containing peer-reviewed papers) and it contains the following sections:

- **Features**: selective short papers within the technical scope of TCVLSI. This section introduces interesting topics related to TCVLSI, and short review/survey papers on emerging topics in the areas of VLSI circuits and systems.
- **Opinions**: Discussions and book reviews on recent VLSI/nanoelectronic/emerging circuits and systems for nanocomputing, and “Expert Talks” to include the interviews of eminent experts for their concerns and predictions on cutting-edge technologies.
- **Updates**: Upcoming conferences/workshops of interest to TCVLSI members, call for papers of conferences and journals for TCVLSI members, funding opportunities and job openings in academia or industry relevant to TCVLSI members, and TCVLSI member news.
- **Outreach and Community**: The “Outreach K20” section highlights integrating VLSI computing concepts with activities for K-4, 4-8, 9-12 and/or undergraduate students. It also features student fellowship information as well a “Puzzle” section for our readership.

We are soliciting contributions to all these four sections. Please directly contact the editors and/or associate editors by email to submit your contributions.

**Submission Deadline:**
All contributions must be submitted by March 1, 2018 in order to be included in the April issue of the letter.

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- **Updates**: Jun Tao, Fudan University, China, taojun@fudan.edu.cn (upcoming conferences, symposia, and workshops, and funding opportunities)
- **Updates**: Himanshu Thapliyal, University of Kentucky, USA, hthapliyal@uky.edu (call for papers and proposals, job openings and Ph.D. fellowships)
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