CALL FOR PAPERS

IEEE Transactions on Sustainable Computing

Special Issue:
"**Beyond the Energy & Performance Scaling Boundaries of Modern Computer Architectures**"

GUEST EDITORS

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TOPIC SUMMARY

State-of-the-art microprocessor and memory chips are conservatively manufactured and operate at pessimistic levels of supply voltage, clock frequency and DRAM refresh rate for addressing the worsening static and dynamic variability in nanometer technologies. Typically, the worst chips being in the weakest corners of the manufacturing process determine the nominal values of the operating conditions although it is widely known that a very large number of chips can safely operate at reduced voltage levels, increased frequencies and relaxed DRAM refresh rates. The margins between the nominal values of the parameters and the actual safe values of individual chips can potentially lead to large savings in energy/power consumption or to large improvements of the performance. Fine-grained tuning of the voltage, frequency and refresh rate settings can also harness the inherent variability among the cores of the same multicore chip or the different DRAM DIMMs of a machine. Different accelerators architectures such as GPUs, FPGAs or other custom accelerator chips already used with state-of-art embedded and high performance systems can be similarly tuned to improve energy and performance efficiency.

An accurate identification and characterization of the voltage, frequency and refresh rate margins and their variability under various workload and environmental conditions can effectively drive software layers solutions for improved energy efficiency or performance, while the correctness/reliability of operation and the required quality-of-service level is preserved. To this aim, diligent communication between the hardware components of a computing system and the system software components that will take workload allocation and system operation integrity decisions are essential. Intelligent margins and variability aware software stack design can maximize the gains, while ensuring robust system operation.

This Special Issue of *IEEE Transactions on Sustainable Computing* will be covering this cross-layer research domain seeking three broad types of contributions: (a) novel methods and flows for the characterization and measurement of the pessimistic design margins and their variability across memory and processor chips and cores, (b) effective prediction and communication/reporting mechanisms to expose hardware margins and variability as well device behavior under non-nominal operating conditions to the software layers and (c) error-resilient software paradigms to harness the exposed margins and variability for improved energy-efficiency and/or performance.

Topics of interest include, but are not limited to:

- Microprocessors, accelerators and memory chips characterization and analytical modeling methodologies under scaled voltage, frequency and refresh rate points and various thermal and other environmental conditions
- Workload characterization at different scales and benchmarking for evaluating operation under scaled operating points in embedded and cyber-physical systems as well as in server and high performance computers.
- Hardware behavior modeling and prediction methods and effective communication and reporting schemes across system layers.
- Variability aware system software design including fault aware runtime and resource management policies for energy and performance efficiency under scaled operating conditions.
- Hardware and software error tolerance methodologies under scaled voltage, frequency, and refresh rate conditions.
- Total cost of ownership (TCO) modelling and analysis frameworks for evaluating the benefits at different scales including cloud and edge infrastructures and personal devices.

IMPORTANT DATES

Submission deadline: **21 February 2018**
First-round notification: **18 April 2018**
Revised papers due: **28 May 2018**
Final notification: **20 July 2018**
Publication Date: **early 2019 (tentative)**

SUBMISSION GUIDELINES

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