Guest Editors’ Introduction: Special Section on Energy Efficient Computing

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From portable devices to data centers, energy consumption has grown to be a major limitation to usability and performance. Energy cost and associated infrastructure also constitute a growing proportion of the expense of building and running a typical data center. Therefore, energy efficient computing has become an active area of research, motivated further by environmental concerns and a desire to limit the impact of computing on the ecosystem.

Unlike many research areas, Energy efficient computing involves all system’s components and design layers. As a result, we often see that specialized forums tend to address only one aspect of the research area, and there isn’t a single forum that adequately covers the large span of topics that touch on power aware computing. Hence the idea behind this special issue: We sought to assemble a special issue that is devoted to the topic at large, and without confining the scope to a particular subtopic.

As a result of the call for papers, we received a total of 44 submissions to this special section. We handled conflict of interest in the traditional way where each of the editors handled the papers with a conflict of interest of the other editor. We obtained at least three reviews for each paper. Only 12 papers survived the first round of revisions and only one of the twelve papers was accepted with minor revisions. The remaining eleven papers went through major revisions and a second round of reviews. Five papers were accepted after the second round with two papers going through a second major revision, and a third round of reviews, after which they were accepted. In total, eight excellent papers appear in this special section and, although there were no attempts to balance the topics of the accepted papers, the eight papers that made it through the review process represent a wide spectrum of interests within power aware computing. This spectrum includes theory, systems, and practice papers, and encompasses different types of systems including high performance systems, servers, real-time systems, and mobile systems. In what follows, we briefly summarize the contributions of each of the eight papers included in this special section.

The paper “Scheduling Precedence Constrained Tasks with Reduced Processor Energy on Multiprocessor Computers,” considers the problems of minimizing schedule length with energy consumption constraints and minimizing energy consumption with schedule length constraints. Scheduling tasks to multiprocessors is generally NP complete, and thus adding energy consumption into the mix adds another dimension of complexity to the problems. This complexity is dealt with by decomposing the problems into subproblems that separate precedence constraints, task scheduling and power budget allocation, leading to three types of power allocation and scheduling heuristics, namely, prepower-determination algorithms, postpower-determination algorithms, and hybrid algorithms. The different algorithms are evaluated and compared through simulation.

In the paper “Synchronization-Aware Energy Management for VFI-based Multicore Real-Time Systems,” the authors investigate scheduling real-time tasks on multicore processors with separate voltage and frequency islands. In addition to the management of computational resources, the authors propose an integrated synchronization-aware framework to appropriately reclaim, preserve, release and steal slack at run time to slow down the execution of tasks within each voltage island, thus reducing the overall energy consumption of the system. Evaluation is also done through simulation.

The goal of the paper “Tiered Memory: An Iso-Power Memory Architecture to Address the Memory Power Wall,” is to reduce the energy consumption of memory systems. It presents a memory architecture that can support more memory capacity for a limited power budget. The architecture is based on dividing the memory into multiple tiers, each set to a different power mode. A formal model is presented for provisioning a memory that is divided into “hot” and “cold” ranks, where the former are kept active (as normal), and the latter are kept in a low-power state. A cold rank is awakened when sufficiently many accesses to it have accumulated or a time-out threshold for delaying cold accesses is reached. Evaluation assuming server-class systems running many virtual machines show that using two-tiers outperforms the conventional single-tier system for an equivalent power budget.

Moving from memory design to processor design, the paper “A Customized Processor for Energy Efficient Scientific Computing,” presents and evaluates a novel architecture specifically designed to tackle identified bottlenecks in GPU architectures when running scientific code. The proposed architecture incorporates special features to deal with efficient back-to-back execution of SIMD floating point operations, memory latency, and control divergence in SIMD execution. Specifically, to improve the power efficiency of dense matrix scientific processors, operations...

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are chained to save computational power, dynamic prefetching is used to improve timeliness, and dual-path execution is employed to increase resource utilization. The performance of the proposed VLIW/SIMD-like architecture is evaluated for scientific applications.

Still in the domain of scientific computing, the paper “Codesign Tradeoffs for High-Performance, Low-Power Linear Algebra Architectures,” recognizes that Level-3 BLAS routines form the basis of a non-negligible fraction of day-to-day computations and describes an accelerator for general matrix-matrix multiplication which can readily be extended to cover other BLAS routines. The design space of the accelerator is thoroughly evaluated with respect to the fundamental tradeoffs and limits in efficiency, measured in "energy per operation". In addition to exposing the sources of inefficiencies in current CPU/GPU systems, the paper demonstrates the flexible customization allowed by the proposed hardware/software codesign approach.

The paper “Exploiting Spatio-Temporal Tradeoffs for Energy-Aware MapReduce in the Cloud,” describes a unique way of scheduling virtual machines to a set of physical servers for MapReduce tasks in a shared cloud environment. The goals are primarily to reduce overall datacenter energy consumption, and secondarily to improve the performance of the tasks when possible. The authors attempt to simultaneously address two problems when mapping virtual machine to physical machine: spatial waste (unused resources on a machine in use) and temporal waste (machines staying online when not doing any useful work). Through a series of experiments using both simulation and a testbed, the authors show that they can achieve their goals using this spatio-temporal tradeoff through a set of algorithms developed as part of this work.

The paper “‘Cool’ Load Balancing for High Performance Computing Data Centers,” deals with methodologies to optimize power consumption of data centers during the execution of tightly coupled parallel applications. The authors demonstrate how changes of the machine room temperature influence the entire energy consumption and runtime of specific applications. In particular a combination of dynamic voltage and frequency scaling and frequency-aware load balancing is used to control the trade-off between machine cooling power and application completion time. Load balancing transparently takes place at the application level and is embedded in the programming tools and run-time support. Charm++ and MPI applications are used as benchmarks to demonstrate the effectiveness of the proposed techniques.

The last paper, “Power Management for Wireless Data Transmission Using Complex Event Processing,” proposes a framework to reduce the energy consumed in mobile devices with the obvious goal of extending the lifetime of the batteries that power them. The framework takes into account the context of an application by adapting the behavior of wireless data transmission to changes in contexts defined by some events and action rules specified by the developers using an XML-based interface. Event processing agents allow for the handling of complex events, the correlation between different events and the application of elaborate action rules to adapt data transmission to traffic patterns and wireless link quality.

Finally, we would like to thank all the authors who submitted papers to this special section and the reviewers who provided the high quality feedback necessary for maintaining the high quality of the accepted papers. We would like also to thank the IEEE staff for their help in facilitating the review process and the editor in chief for making this special section possible. We hope that you will enjoy reading the high quality papers included in this special section.

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