Table of Contents

Message from the Steering Committee Chair ................................................................. xv
Welcome Message ........................................................................................................... xvi
Welcome Message from the General Chair ................................................................. xvii
Welcome Message from the Program Chairs .............................................................. xix
Message from the President, VLSI Society of India .................................................. xxi
Message from the Tutorial Co-Chairs ........................................................................ xxii
Message from the User/Designer Track Chair ........................................................... xxiii
VLSI Design Conference Steering Committee (2013) .................................................... xxiv
VLSI Design 2013 Conference Committee ................................................................... xxv
Program Committee .................................................................................................... xxviii
Plenary Talk Abstracts ................................................................................................... xxxiv
About the Cover from the Publication Co-Chairs ........................................................ xlv
VLSI Design Conference History ................................................................................ xlvii
Embedded Systems Design Conference History ......................................................... xlviii
Conference Program ................................................................................................. li
Call for Papers — VLSI Design and Test Symposium (VDAT 2014) .............................. li

Tutorials

Tutorial T1: Ambient Intelligence through Internets-of-Things—An Application
Development Approach .................................................................................................. 1

Anil Kumar Gupta, Anand Singh, and Vineeta Yadav

Tutorial T2A: Scheduling Issues in Embedded Real-Time Systems .............................. 2

Parmesh Ramanathan

Tutorial T2B: Cost / Application / Time to Market Driven SoC Design
and Manufacturing Strategy .......................................................................................... 3

Barun Kumar De, Anupam Chattopadhyay, and Ansuman Banerjee
Session A2: SAT Application

Debug Automation for Synchronization Bugs at RTL .................................................................44

Mehdi Dehbashi and Görschwin Fey

Techniques to Improve the Efficiency of SAT Based Path Delay Test Generation ........................................50

Kun Bian, D.M.H. Walker, and Sunil P. Khatri

SAT-Based Test Pattern Generation with Improved Dynamic Compaction ........................................56

Alexander Czutro, Sudhakar M. Reddy, Ilia Polian, and Bernd Becker

Efficient SAT-Based Circuit Initialization for Larger Designs ...........................................................62

Matthias Sauer, Sven Reimer, Sudhakar M. Reddy, and Bernd Becker

Session A3: Design Verification

A Coverage Guided Mining Approach for Automatic Generation of Succinct Assertions .......................................................68

David Sheridan, Lingyi Liu, Hyungsul Kim, and Shobha Vasudevan

Effective Liveness Verification Using a Transformation-Based Framework ........................................74

Pradeep Kumar Nalla, Raj Kumar Gajavelly, Hari Mony, Jason Baumgartner, and Robert Kanzelman

Formal Verification and Debugging of Array Dividers with Auto-correction Mechanism .................................80

M.H. Haghbayan, B. Alizadeh, P. Behnam, and S. Safari

All-SAT Using Minimal Blocking Clauses .........................................................................................86

Yinlei Yu, Pramod Subramanyan, Nestan Tsiskaridze, and Sharad Malik

Session A4: Test Generation

CryptIP: An Approach for Encrypting Intellectual Property Cores with Simulation Capabilities ...........................................92

Spencer Millican, Parameswaran Ramanathan, and Kewal Saluja

A Cube-Aware Compaction Method for Scan ATPG .................................................................................98

Sharada Jha, Kameshwar Chandrasekar, Weixin Wu, Ramesh Sharma, Sanjay Sengupta, and Sudhakar M. Reddy

Scalable Test Generation by Interleaving Concrete and Symbolic Execution ............................................104

Xiaoke Qin and Prabhat Mishra

Application of Test-View Modeling to Hierarchical ATPG ........................................................................110

Rahul Shukla, Phong Loi, Ken Pham, Arie Margulis, Kathy Yang, and Nagesh Tamarapalli
Session A5: Reliable Circuits

A New Sensitivity-Driven Process Variation Aware Self-Repairing Low-Power SRAM Design .......................................................... 116
  Nandakishor Yadav, Sunil Dutt, and G.K. Sharma

Timing Variation Adaptive Pipeline Design: Using Probabilistic Activity Completion Sensing with Backup Error Resilience ........................................ 122
  Jayaram Natarajan, Sahil Kapoor, Debesh Bhatta, Abhijit Chatterjee, and Adit Singh

A Novel Low Power Error Detection Logic for Inexact Leading Zero Anticipator in Floating Point Units ................................................ 128
  B. Naveen Kumar Reddy, M. Chandra Sekhar, Sreehari Veeramachaneni, and M.B. Srinivas

Better-than-Worst-Case Timing Design with Latch Buffers on Short Paths .......................................................... 133
  Ravi Kanth Uppu, Ravi Tej Uppu, Adit D. Singh, and Ilia Polian

Session A6: Memory

Pipelined Non-strobed Sensing Scheme for Lowering BL Swing in Nano-scale Memories .................................................. 139
  Sudhanshu Khanna, Satyanand V. Nalam, and Benton H. Calhoun

Energy Efficient Memory Decoder Design for Ultra-low Voltage Systems .......................................................... 145
  K.R. Viveka and Bharadwaj Amrutur

A 500 mV to 1.0 V 128 Kb SRAM in Sub 20 nm Bulk-FinFET Using Auto-adjustable Write Assist .......................................................... 150
  Prashant Dubey, Gaurav Ahuja, Vaibhav Verma, Sanjay Kumar Yadav, and Amit Khanuja

Minimizing Power and Skew in VLSI-SoC Clocking with Pulsed Resonance Driven De-skewing Latches .......................................................... 156
  Ignatius Bezzam and Shoba Krishnan

Session B1: Real-Time Systems

Efficient Two-Phase Approaches for Branch-and-Bound Style Resource Constrained Scheduling .......................................................... 162
  Mingsong Chen, Fan Gu, Lei Zhou, Geguang Pu, and Xiao Liu

Inserting Placeholder Slack to Improve Run-Time Scheduling of Non-preemptible Real-Time Tasks in Heterogeneous Systems .......................................................... 168
  Hsiang-Kuo Tang, Parmesh Ramanathan, and Katherine Morrow

Hardware Implementation of Real-Time, High Performance, RCE-NN Based Face Recognition System .......................................................... 174
  Santu Sardar and K. Ananda Babu
Session B2: Embedded Platform

EME Electric Supervision Embedded on Gas Panel with Microshock Dangerousness
Degree ........................................................................................................................................................................180

    Marcelo Trindade Rebonatto, Fabiano Passuelo Hessel,
    and Luiz Eduardo Schardong Spalding

Design of AFE and PWM Drive for Lithium-Ion Battery Management System
for HEV/EV System ...................................................................................................................................................186

    Sudhakar Singamala, Mandfed Brandl, Sandeep Vernekar, Veereshbabu Vulligadala,
    Ravikumar Adusumalli, and Vijay Ele

Process Disturbance Analyzer for Nuclear Reactors ..............................................................................................192

    E.M.T. Sirisha, T. Sridevi, and D. Thirugnana Murthy

Design and Implementation of Safety Logic with Fine Impulse Test System for
a Nuclear Reactor Shutdown System .........................................................................................................................198

    Manoj Kumar Misra, N. Sridhar, and D. Thirugnana Murthy

Session B3: Architectures

Performance and Power Benefits of Sharing Execution Units between a High
Performance Core and a Low Power Core .................................................................................................................204

    Rance Rodrigues, Israel Koren, and Sandip Kundu

Process Synchronization in Multi-core Systems Using On-Chip Memories ..............................................................210

    Arun Joseph and Nagu R. Dhanwada

TECS: Temperature- and Energy-Constrained Scheduling for Multicore Systems ..................................................216

    Xiaoke Qin and Prabhat Mishra

Challenges in Implementing Cache-Based Side Channel Attacks on Modern
Processors ..................................................................................................................................................................222

    Jyoti Gajrani, Pooja Mazumdar, Sampreet Sharma, and Bernard Menezes

Session B4: Network-on-Chip

Tiny NoC: A 3D Mesh Topology with Router Channel Optimization for Area
and Latency Minimization ..........................................................................................................................................228

    César Marcon, Ramon Fernandes, Rodrigo Cataldo, Fernando Grando, Thais Webber,
    Ana Benso, and Leticia B. Poehls

NoC Scheduling for Improved Application-Aware and Memory-Aware Transfers
in Multi-core Systems .................................................................................................................................................234

    Tejas Pimpalkhute and Sudeep Pasricha

CARM: Congestion Adaptive Routing Method for On Chip Networks ......................................................................240

    Manoj Kumar, Vijay Laxmi, Manoj Singh Gaur, Seok-Bum Ko, and Mark Zwolinski
Knowledge-Guided Methodology for Third-Party Soft IP Analysis ................................................................. 246
Bhanu Singh, Arunprasath Shankar, Francis Wolff, Daniel Weyer, Christos Papachristou, and Bhanu Negi

Session B5: MPSoCs
Pre-mapping Algorithm for Heterogeneous MPSoCs ....................................................................................... 252
César Marcon, Thais Webber, Leticia B. Poehls, and Igor K. Pinotti
Efficient QR Decomposition Using Low Complexity Column-wise Givens Rotation (CGR) ........................................... 258
Farhad Merchant, Anupam Chattopadhyay, Ganesh Garga, S.K. Nandy, Ranjani Narayan, and Nandhini Gopalan
Temperature Minimization Using Power Redistribution in Embedded Systems ...................................................... 264
Rehan Ahmed, Parameswaran Ramanathan, and Kewal K. Saluja
Process Variation Aware Synthesis of Application-Specific MPSoCs to Maximize Yield ........................................ 270
Nishit Kapadia and Sudeep Pasricha

Session B6: Embedded Systems
Hard versus Soft Software Defined Radio ............................................................................................................. 276
Wim Meeus, Tom Vander Aa, Praveen Raghavan, and Dirk Stroobandt
Interfacing Synchronous and Asynchronous Domains for Open Core Protocol ................................................... 282
Vikas S. Vij, Raghu Prasad Gudla, and Kenneth S. Stevens
Control Mechanism to Solve False Blocking Problem at MAC Layer in Wireless Sensor Networks .......................... 288
Brajendra K. Singh, Kemal E. Tepe, and Mohammed A.S. Khalid
Architecture for Blocking Detection in Wireless Video Source Authentication ................................................... 294
Amit Pande, Shaxun Chen, Prasant Mohapatra, and Gaurav Pande

Session C1: FPGA
A Novel Architecture for FPGA Implementation of Otsu’s Global Automatic Image Thresholding Algorithm ................................................................. 300
J.G. Pandey, A. Karmakar, C. Shekhar, and S. Gurunarayanan
Accelerating Genome Assembly Using Hard Embedded Blocks in FPGAs ......................................................... 306
B. Sharat Chandra Varma, Kolin Paul, and M. Balakrishnan
A Hardware Intensive Approach for Efficient Implementation of Numerical Integration for FPGA Platforms .................. 312
Burhan Khurshid and Roozie Naz Mir
Embedded Complex Floating Point Hardware Accelerator .................................................................................... 318
Amin Ghasemazar, Mehran Goli, and Ali Afzali-Kusha
Session C2: Low-Power Design

A Power Efficient Video Encoder Using Reconfigurable Approximate Arithmetic Units ................................................................. 324

Arnab Raha, Hrishikesh Jayakumar, and Vijay Raghunathan

QUICKRECALL: A Low Overhead HW/SW Approach for Enabling Computations across Power Cycles in Transiently Powered Computers .................................................................................................................. 330

Hrishikesh Jayakumar, Arnab Raha, and Vijay Raghunathan

Configurable Systolic Matrix Multiplication .................................................................................................................................................. 336

Parastoo Kamranfar, S. Ali Shahabi, Ghazaleh Vazhbakht, and Zainalabedin Navabi

ProCA: Progressive Configuration Aware Design Methodology for Low Power Stochastic ASICs ............................................................................................................................................................................ 342

Neel Gala, V.R. Devanathan, Karthik Srinivasan, V. Visvanathan, and V. Kamakoti

Session C3: Digital Design

Hardware Efficient VLSI Architecture for 3-D Discrete Wavelet Transform ........................................................................................................... 348

Anand Darji, Saurabh Shukla, S.N. Merchant, and A.N. Chandorkar

Design and Implementation of High Throughput and Area Efficient Hard Decision Viterbi Decoder in 65nm Technology ................................................................. 353

Narayan V. Sugur, Saroja V. Siddamal, and Samba Sivam Vemala

Scalable Low Power FFT/IFFT Architecture with Dynamic Bit Width Configurability ................................................................. 359

Sundarajan Rangachari, Jaiganesh Balakrishnan, and Nitin Chandrachoodan

A Decimal/Binary Multi-operand Adder Using a Fast Binary to Decimal Converter ........................................................................................................... 365

Ch. Santosh Varma, Syed Ershad Ahmed, and M.B. Srinivas

Session C4: Physical Design

Global Routing Using Monotone Staircases with Minimal Bends ........................................................................................................... 369

Bapi Kar, Susmita Sur-Kolay, and Chittaranjan Mandal

Delete and Correct (DaC): An Atomic Logic Operation for Removing Any Unwanted Wire .................................................................................................................................................................................. 375

Xing Wei, Tak-Kei Lam, Xiaoqing Yang, Wai-Chung Tang, Yi Diao, and Yu-Liang Wu

On Manufacturing Aware Physical Design to Improve the Uniqueness of Silicon-Based Physically Unclonable Functions ........................................................................................................... 381

Raghavan Kumar, Siva Nishok Dhanuskodi, and Sandip Kundu

Obstacle Avoiding Rectilinear Clock Tree Construction with Skew Minimization ........................................................................................................... 387

Partha Pratim Saha and Tuhina Samanta

Layout-Aware Delay Variation Optimization for CNTFET-Based Circuits ........................................................................................................... 393

Matthias Beste, Saman Kiamehr, and Mehdi B. Tahoori
Session C5: Modeling and Simulation
Leakage Modeling for Devices with Steep Sub-threshold Slope Considering Random Threshold Variations ..........................................................399
Ayan Paul, Chaitanya Kshirsagar, Sachin S. Sapatnekar, Steven Koester, and Chris H. Kim

Small Signal Nonquasi-static Model for Common Double-Gate MOSFETs Adapted to Gate Oxide Thickness Asymmetry .........................................................405
Neha Sharan and Santanu Mahapatra

Analytical Modeling of Sub-onset Current of Tunnel Field Effect Transistor ..........................................................411
Parmanand Singh, Vivek Asthana, Radhakrishnan Sithanandam, Anand Bulusu, and Sudeb Das Gupta

Statistical Modeling of Glitching Effects in Estimation of Dynamic Power Consumption ..........................................................415
Michael Meixner and Tobias G. Noll

Session C6: Modeling and Analysis
BSIM6—Benchmarking the Next-Generation MOSFET Model for RF Applications ..........................................................421
Anupam Dutta, Saurabh Sirohi, Tamilmani Ethirajan, Harshit Agarwal, Yogesh Singh Chauhan, and Richard Q. Williams

Analysis of Nanoscale Strained-Si/SiGe MOSFETs including Source/Drain Series Resistance through a Multi-iterative Technique ..........................................................427
Amrita Kumari and Subindu Kumar

An ABCD Parameter Based Modeling and Analysis of Crosstalk Induced Effects in Multiwalled Carbon Nanotube Bundle Interconnects ..........................................................433
Manodipan Sahoo, Prasun Ghosal, and Hafizur Rahaman

Performance Optimization and Parameter Sensitivity Analysis of Ultra Low Power Junctionless MOSFETs ..........................................................439
Mukta Singh Parihar and Abhinav Kranti

Session D1: RF Circuits
Improvements to Negative-C Compensation Based Amplifiers for Broadband Applications ..........................................................444
Rajesh Cheeranthodi, Santhosh Madhavan, Umesh K. Shukla, and Giri N. Rangan

An Adaptive Inductorless Continuous Time Equalizer for Gigabit Links in 0.13 um CMOS ..........................................................450
Sushrant Monga and Shouri Chatterjee

On Dependence of Amplitude Noise versus Offset Frequency in LC Oscillators ..........................................................455
R. Sivaramakrishna and Shalabh Gupta
A 1 V, Sub-mW CMOS LNA for Low-Power 1 GHz Wide-Band Wireless
Applications .........................................................................................................................460

Arunkumar Salimath, Pradeep Karamcheti, and Achintya Halder

Session D2: LP Circuits
Low Power Single Amplifier Voltage Regulator ....................................................................466

Sanjay Kumar Wadhwa, Jaideep Banerjee, and Rakesh Kumar Gupta
Forward Body Biased Adiabatic Logic for Peak and Average Power Reduction
in 22nm CMOS ..................................................................................................................470

Matthew Morrison and Nagarajan Ranganathan
FinFET Logic Circuit Optimization with Different FinFET Styles: Lower Power
Possible at Higher Supply Voltage ..................................................................................476

Sourindra Chaudhuri and Niraj K. Jha
Operand Isolation with Reduced Overhead for Low Power Datapath Design ..................483

Lokesh Siddhu, Amit Mishra, and Virendra Singh
High-Speed, Low-Power Quasi Delay Insensitive Handshake Circuits Based
on FinFET Technology ......................................................................................................489

Mohammad Yousef Zarei, Mahdi Mosaffa, and Siamak Mohammadi

Session D3: MEMS/Biochips
Active Cooling Technique for Efficient Heat Mitigation in 3D-ICs ........................................495

Pramod Kaddi, Basireddy Karunakar Reddy, and Shiv Gobind Singh
Improved Design Methodology for the Development of Electrically Actuated MEMS
Structures ...............................................................................................................................499

AVSS Prasad, K.P. Venkatesh, Rudra Pratap, and Navakanta Bhat
Correctness Checking of Bio-chemical Protocol Realizations on a Digital Microfluidic
Biochip ....................................................................................................................................504

Sukanta Bhattacharjee, Ansuman Banerjee, Krishnendu Chakrabarty,
and Bhargab B. Bhattacharya
A Novel Wire Planning Technique for Optimum Pin Utilization in Digital
Microfluidic Biochips .............................................................................................................510

Pranab Roy, Samadrita Bhattacharya, Rupam Bhattacharyya, Firdousi Jamil Imam,
Hafizur Rahaman, and Parthasarathi Dasgupta

Session D4: Analog Circuits I
Output Impedance as Figure of Merit to Predict Transient Performance for Embedded
Linear Voltage Regulators ....................................................................................................516

Saurabh Kumar Singh and Nitin Bansal
A Time-Based Low Voltage Body Temperature Monitoring Unit ........................................522

Karthik Ramkumar Jeyashankar, Makrand Mahalley, and Bharadwaj Anrutur
Trimless, PVT Insensitive Voltage Reference Using Compensation of Beta and Thermal Voltage .................................................................................................................. 528
   Hande Vinayak Gopal and Maryam Shojaei Baghini

A Low Power CMOS Imager Based on Distributed Compressed Sensing .................................................................................. 534
   Bhuvanan Kaliannan and Vijaya Sankara Rao Pasupureddi

Session D5: Emerging Technologies

All Optical Reversible Multiplexer Design Using Mach-Zehnder Interferometer .................................................................................. 539
   Kamalika Datta and Indranil Sengupta

Circuit for Reversible Quantum Multiplier Based on Binary Tree Optimizing Ancilla and Garbage Bits ............................................................................................................. 545
   Saurabh Kotiyal, Himanshu Thapliyal, and Nagarajan Ranganathan

Design of Dedicated Reversible Quantum Circuitry for Square Computation .......................................................................................... 551
   H.V. Jayashree, Himanshu Thapliyal, and Vinod Kumar Agrawal

An Optimized Design of Reversible Quantum Comparator .......................................................................................................................... 557
   P. Sai Phaneendra, Chetan Vudadha, V. Sreehari, and M.B. Srinivas

Session D6: Analog Circuits II

Light Load Efficiency Improvement in High Frequency DC-DC Buck Converter Using Dynamic Width Segmentation of Power MOSFET .................................................................. 563
   N.J. Metilda Sagaya Mary, Ashis Maity, and Amit Patra

Histogram Based Deterministic Digital Background Calibration for Pipelined ADCs ........................................................................ 569
   Chithira Ravi, T. Rahul, and Bibhudatta Sahoo

A Power Efficient Fully Differential Back Terminated Current-Mode HDMI Source .................................................................................. 575
   R. Gopikrishnan, Vijaya Sankara Rao Pasupureddi, and Govindarajulu Regeti

An Adaptive Body-Biased Clock Generation System in 28nm CMOS .......................................................................................................... 580
   Makarand Shirasgaonkar, Roxanne Vu, Deborah Dressler, Nhat Nguyen, Kambiz Kaviani, and Yueyong Wang

Author Index .................................................................................................................................................................................. 584