Tutorial T7A

Techniques for Network-on-Chip (NoC) Design and Test

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Abstract

System-on-Chip (SoC) is a paradigm for designing today’s integrated circuit (IC) chips that puts an entire system onto a single silicon floor (instead of printed circuit boards containing a number of chips accomplishing the system task). With the increasing number of cores integrated on such a chip, on-chip communication efficiency has become one of the key factors in determining the overall system performance and cost. The communication medium used in most of the modern Systems-on-Chip (SoCs) is shared global bus. In spite of fairly simple structure, extensibility, and low area cost of bus, at the system level, it can be used for only up to tens of cores on a single chip. The restriction comes mainly due to the following reasons – non-scalable wire delay with technology shrinking, non-scalable system performance with number of cores attached, decrease in operating frequency with each additional core attached, high power consumption in long wires, etc. Network-on-Chip (NoC) is an emerging alternative that overcomes the abovementioned bottlenecks for integrating large number of cores on a single SoC. NoC is a specific flavor of interconnection networks where the cores communicate with each other using a router based packet switched network. Interconnection networks have been studied for more than last two decades and a solid foundation of design techniques has been reported in the literature. NoC is today becoming an emerging research and development topic including hardware communication infrastructure design, software and operating system services, CAD tools for NoC synthesis, NoC testing, and so on.

This tutorial aims at covering the important aspects of NoC design – communication infrastructure design, communication methodology, evaluation framework, mapping of applications onto NoC etc. Apart from these, it also proposes to focus on other upcoming NoC issues, such as, NoC testing, reconfiguration, synthesis and 3-D NoC design.

Speaker Biographies

Santanu Chattopadhyay received his BE degree in Computer Science and Technology from Calcutta University (B.E. College) in 1990. He received his M.Tech degree in Computer and Information Technology from Indian Institute of Technology, Kharagpur in 1992. He also did his PhD from the same institute in 1996 in Computer Science and Engineering. He is currently a Professor in the Dept. of Electronics and Electrical Communication Engineering, IIT Kharagpur. His research interests include Network-on-Chip Design and Test, Low-power VLSI Design and Test, Fault Diagnosis, etc. He is in the Editorial Board of the IET Journals – Circuits, Devices & Systems. He has published more than 150 technical papers in reputed refereed international journals and conferences. He has coauthored a book on Additive Cellular Automata – Theory and Applications (Vol. 1),...
published by the IEEE Computer Society Press, USA, and has written text books on *Compiler Design, System Software, Embedded System Design (Ed.2)*, published by the PHI Learning, India. He has received the *Supreme Engineering Award, 2012*, for being judged the *Best Faculty in Engineering*. He has presented several tutorials on related topics, earlier.