Tutorial 5

Design challenges in sub-100nm high performance microprocessors

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Abstract

In future CMOS technology generations, device dimensions, supply and threshold voltages will have to continually scale to sustain performance increase, limit energy consumption, control power dissipation, and maintain reliability. These scaling requirements pose several device and circuit design challenges for high performance microprocessors. In scaled technologies, minimizing impact of process variation on circuits and total system power become more vital. This tutorial will examine the challenges stemming from scaling and increased levels of integration. We will take a close look at the past trends in technology scaling of various microprocessors and project them into the future while identifying the key barriers stemming from device physics, circuit functionality, heat removal, power delivery, battery life, and soft error rate. Device challenges including gate leakage, junction tunneling, junction depth scaling, parasitic series resistance, and short channel effects have to be addressed.

Microprocessor frequencies are increasing every generation from additional architectural and circuit complexity, which demands higher level of integration and die size increase. Increase in complexity leads to increase in power consumption and current delivery requirement.
Furthermore, on-chip and package interconnect parasitics do not scale well with technology. A combination of device scaling and increased integration results in increased power dissipation and higher power density. We will present these scaling challenges in detail and propose solutions to address them including power efficient design choices.

To address these scaling challenges, devices, circuits and design methodologies need to evolve. On the device front, maintaining good device aspect ratio, by scaling gate oxide thickness is important for controlling short channel effects. With the silicon dioxide gate dielectric thickness approaching scaling limits due to rapid increase in gate tunneling leakage current, researchers have been exploring several alternatives, including the use of high permittivity gate dielectric, metal gate and novel device structures. Circuit based techniques, on the other hand, include adaptive threshold voltage and supply voltage schemes for parameter variation tolerance. In leakage dominated technologies it also becomes crucial to employ circuit techniques to reduce active and standby leakage powers. We will discuss various solutions such as sleep transistors and body bias. Design methodologies to incorporate the above solutions into large microprocessors will be presented. Advanced CAD tools are required that incorporate techniques such as statistical based methodologies as well as accurate leakage power prediction models which take into account within-die parameter variation.

Further, we will cover power reduction strategies applicable globally to a microprocessor design. These include addressing RC delay of long on-chip interconnects using coding techniques and meeting the need for larger amounts of caches by using novel on-die memory structures, such as 1-T DRAM cells. Additionally, general-purpose microprocessors are rapidly becoming overwhelmed with the burden of processing special purpose tasks. We will present the benefits of special purpose computation to achieve better power efficiency by highlighting two application domains - network and signal processing.

**Biography**

Siva Narendra received the B.E. degree from Government College of Technology, Coimbatore, India, in 1992, the M.S. degree from Syracuse University, Syracuse, NY, in 1994, and the Ph.D. degree from Massachusetts Institute of Technology, Cambridge, in 2002. He has been with Intel Laboratories since 1997, where his research areas include low voltage MOS analog and digital circuits and impact of MOS parameter variation on circuit design. He has authored or co-authored 24 papers and has 27 issued and 16 pending patents in these areas. Dr. Narendra is an Adjunct Faculty with the Department of Electrical and Computer Engineering, Oregon State University, Corvallis. He is an Associate Editor for the IEEE Transactions on VLSI systems and a member of the ISLPED, ISQED and ISSCC Student Design Contest Technical Program Committees.

Vasantha Erraguntla received a Bachelors degree in Electrical Engineering from Osmania University, India and a Masters in Computer Engineering from University of Southwestern Louisiana. She joined Intel in 1991 and worked on the high-speed router technology for the Teraflop machine. She then joined Design Technology team validating performance verification tools for high-speed designs. For the last 6 yrs, Vasantha has been engaged in a variety of
advanced prototype design activities at Intel Laboratories, implementing and validating research ideas in the areas of in high performance & low power circuits and high speed signaling. She has co-authored 7 papers and has 4 patents pending in this area. Vasantha is also a member of IEEE.

James W. Tschanz received the B.S. degree in computer engineering in 1997, and the M.S. degree in electrical engineering in 1999, both from the University of Illinois at Urbana-Champaign. Since 1999 he has been a circuits researcher at Intel Laboratories in Hillsboro, OR. His research interests include low-power digital circuits, design techniques, and methods for tolerating parameter variations. He is an adjunct faculty member at the Oregon Graduate Institute in Beaverton, OR, and has authored several papers and patents pending.

Nitin Borkar received M.Sc. Physics in 1982 from University of Bombay and MSEE from Louisiana State University in 1985. He joined Intel Corporation in 1986, where he worked on the design of the i960 family of embedded microcontrollers. In 1990, he joined the i486DX2 microprocessor design team and led the design and the performance verification program. After successful completion of the i486DX2 development, Nitin worked on high-speed router technology for the Teraflop machine. Nitin now leads the prototype design team in Intel Laboratories, implementing and validating research ideas in the areas of in high performance - low power circuits and high speed signaling. He has co-authored several papers and has 4 issued and 6 patents pending in this area.