Tutorial T4

Specification and Design of Multi-Million Gate SOCs

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Abstract

Recent advances in semiconductor technology have made it possible to integrate multi million transistors on a single chip, design and verification teams face several challenges managing the complexity. Some of these challenges include, specification and verification at the functional level, closing early on the system level architecture, extensive simulations of the hardware and software components and finalizing the path to implementation of the entire SOC.

This tutorial will cover the state-of-the-art in specification, design and verification techniques. It will benefit design engineers, managers, researchers and students who are interested in understanding these new modeling, design and verification paradigms. This full-day tutorial is structured into five major parts.

(a) System level design challenges from a designers perspective
(b) Specification languages for system level design that includes
(c) Functional and architectural modeling and verification
(d) Platform based design concepts
(e) Path from specification to implementation.

An overview of the real challenges faced by system level designers will be presented with examples. The weaknesses of traditional design methods will be highlighted, thereby motivating the need for newer system level design tools and methodologies.

Several specification languages are evolving to meet the challenges of SOC design. These languages focus on increasing the level of abstraction, thereby improving simulation performance and enabling SOC design. Languages such as SystemC, SpecC, CycleC and Superlog represent different approaches to address the system specification problem. We present an overview of these languages and discuss some of the specific properties that enable SOC design.

We will cover important aspects of system level modeling and verification: These include modeling and verification at the functional, transactional and RTL levels. Initially, the entire system functionality is modeled in order to analyze system level performance. In general this requires heterogeneous modeling methods involving several models of computation. Then the architecture details are finalized. Transaction level modeling techniques are used to obtain high simulation...
performance. This enables early architecture closure and provides a platform for software development.

One popular method to manage SOC design complexity is to define a platform, which is an abstraction that embodies the lower level details. Typical platforms include a programmable processor, a communications and memory architecture, and possibly a DSP. Such a platform along with an associated RTOS, forms the basis for the SOC design. We will discuss commercial platforms that focus on lower power.

The path to implementation from system level specification can be in any one of three domains: software; hardware; or hardware/software. We will discuss methodologies available for each of these implementations, and will discuss the techniques that are used to optimize parameters such as target performance, low power consumption and cost. We focus on ASIPs for software realization and synthesis techniques for hardware realization. Finally in the hardware/software implementation we will show the procedures that can lead to single/multi processor systems and ASIPs.

Ramesh Chandra is an engineering manager in the Advanced Systems Technology Division in ST Microelectronics in San Diego California. He received his B.E in Electronics Engineering and a MSc in Mathematics from the Birla Institute of Technology in Pilani, India. His current interests include system design methodologies, architectures, embedded processor design.

Dr. Joerg Henkel is with the NEC Laboratories America, Princeton, NJ, where he has initiated various projects related to low power system-level design issues and high performance embedded architectures. He received his MS and PhD both from the Technical University of Braunschweig, Germany. Dr. Henkel has published around 60 technical papers in the areas of low power design, platform-based design and hw/sw co-design. Dr. Henkel is a Senior Member of the IEEE.

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Prof. Sri Parameswaran is an associate professor at the University of New South Wales. He received his Bachelors in Electrical and Computer Systems Engineering at Monash University and his PhD at University of Queensland in Australia. He has been a consultant to a wide variety of high tech companies and the Asian Development Bank. His research interests include, System Level Synthesis, Low power design, Estimation for nanometer technologies, and ASIPs.

Dr Loganath Ramachandran is a senior engineering manager in the System Level Design group in Synopsys based in Mtn View, California. He has also worked at LSI Logic (Milpitas) and Texas Instruments (India). Dr Ramachandran received his Bachelors in Electrical Engg from I.I.T. Madras and his MS and PhD in Computer Science from University of California, Irvine. His research interests include, behavioral and system level synthesis, functional and architectural verification. He is also a member of the Verification Working Group in Open SystemC Initiative (OSCI) focusing on verification extensions to the SystemC language.