Tutorial: Next Generation Network Processors

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Network Processors are highly specialized processors geared towards providing sophisticated packet processing functions in data networking application. Sophisticated packet processing entails packet extraction from multiprotocol encapsulations, packet classification for routing and Quality of Service (QoS) determination as well as security filtering, packet queueing, scheduling and buffer management for differentiated services support and packet modification for fragmentation, encryption, error detection, tunneling, segmentation and reassembly, and other transcoding purposes. By providing these packet processing functions, network processors constitute the very core of a network elements ability to support a diverse set of data networking applications such as Internet Telephony, IP VPN and Mobile IP.

Traditionally, RISC based CPUs have been employed for handling packet processing functions. The primary advantage of using RISC based CPUs has been ease of programmability. However, as network interface speeds have increased, sequential RISC processor bus speeds and clock speeds have not typically scaled to keep up. Another approach has been to use ASICs that use specialized hardware to meet the line rate scaling needs. However, ASICs tend to have limited programmability, resulting in long turn around times to spin next generation silicon as feature and function requirements evolve. Next generation network processors are seeking to overcome the trade-off between flexibility and performance by deploying new programmable architectures that scale to gigabit speeds and beyond.

This tutorial will be divided into four parts.

Part I will cover the essential packet processing functions required in a typical network processor such as:

* Packet extraction from multiprotocol encapsulations
  - IPv4/Ethernet DIX Packets
  - IPv4/Ethernet 802.3 Packets
  - IPv4/PPP/POS Packets
  - IPv4/ATM Packets
  - IPv4/FR Packets
  - IPv4 Tunneling

* Packet classification for
  - IP Route Lookup
  - QoS determination based on Multi-field
  - QoS determination on DSCP
  - Security filtering
  - Flow identification
  - Policing

* Packet Queueing for
  - Scheduling (WF2Q, DWRR)
- Buffer Management (RED, WRED, EPD, PPD)
- Fairness (Stochastic, Deterministic)

* Packet Modification for
  - Fragmentation
  - Encryption/Decryption
  - Error Detection (CRC)
  - DSCP marking
  - Encapsulation/Decapsulation (tunnels)
  - Segmentation and Reassembly (SAR)
  - Other transcoding functions

* Packet Metering
  - Statistics collection
  - Billing
  - Load Balancing

* Packet Exceptions and Control Packets Handling
  - IPv4 Options
  - Layer 2 Control Packets
  - Layer 3 Control Packets
  - Layer 4 Control Packets

Part II will cover traditional RISC-based as well as next generation approach to network processor architectures. It will explain the limitations of the traditional RISC-based architectures in meeting the objective of high speed network processing while retaining the flexibility of programming. Traditional approaches covered will include techniques such as:

* Functional Partitioning
* Parallel Processing
* Cache Optimization
* Bus Optimization
* Network Function Acceleration Co-processors

The scaling limits of each of these techniques will be discussed. Next generation network processor architectures that are non-RISC based will be described. These approaches employ techniques such as:

* Sequential Processing
* Pipelined Processing
* Specialized Function Blocks
* Parallel Processing
* I/O Optimization

Part III will provide a survey of currently available network processors in the industry from some leading vendors such as:

* Agere
A brief comparative assessment will be provided based on functions, and features supported and various architectural approaches adopted.

Part IV will cover applications that are facilitated by network processor functionality in network elements that are deployed in various data networking scenarios. The applications covered will include:

* Internet Telephony
* IP VPN
* Mobile IP

Deepak Kataria is a Systems Architect in the Network Processor and Switching organization of Lucent Microelectronics. He is currently engaged in developing system architectures and applications that are based on protocol independent OC192 port cards used with protocol independent terabit fabrics. Prior to this he worked on OC12 and OC48 protocol independent traffic manager and network processor solutions. He was a Systems Architect in Data Networking Systems organization of Lucent Technologies working on traffic management and resource management architectures for the Packetstar ATM edge switch. He was also responsible for formulating and promulgating ATM traffic management standards and intellectual positions for Lucent Technologies in the ATM Forum. Deepak holds a B.S. in Electronics & Communications Engineering and M.S. and Ph.D. in Electrical Engineering from Rutgers University, New Jersey, USA.