Tutorial: Low-Power Mobile Wireless Communication System Design: Protocols, Architectures, and Design Methodologies

Presenters

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The demand for ubiquitous information access and manipulation (anytime, anywhere computing and communications) has created significant challenges and opportunities for the semiconductor industry. The revenue from wireless voice/data handsets is expected to exceed that from PCs in the near future, and the use of wireless internet access is expected to overtake fixed internet access in the next few years.

The above trends make it important for semiconductor vendors, electronic system design houses, and tools companies to focus their efforts on addressing the challenges encountered in the design of mobile wireless communication systems. One of the most important criteria in the design of such systems is to maximize the battery life, since it directly impacts the duration and extent of mobility. The increasing complexity of wireless communication protocols, increasing performance requirements due to the need for bandwidth, and relatively slow growth in battery technology, make it critical to consider power consumption issues during the design of the protocols and system architecture. This tutorial will survey power-conscious design of the protocols, system architectures, and design methodologies and tools, used in wireless communications systems.

The first part of the tutorial will present an introduction to the different components of radio architectures used in wireless communication systems. We will describe power issues and reduction techniques that can be employed in various parts, including source coding, channel coding, modulation, and power amplification, and various layers of the protocol stack. Since minimizing the total energy consumption does not exactly translate into maximum battery life, we will also examine battery-friendly schemes for communication protocols.

The second part will survey low-power system architectures for mobile communications systems. We will describe low-power tradeoffs and features available in various system components, as well as system-level integration and co-design tradeoffs. Examples of IP cores currently available in the market will be used to illustrate the issues involved in selecting and designing with low-power system components. We will present various embedded processor architectures that are suitable for mobile communications systems and describe the architectural techniques that they employ for lowering power consumption.

The last part of the tutorial will focus on system-level design methodologies and tools for power analysis and reduction. Topics covered will include system-level power estimation and profiling, HW/SW partitioning and mapping for low-power, low-power embedded software, dynamic voltage and performance management strategies, memory and I/O optimizations, power issues in bus architectures, system-level power management, and battery-friendly system design.

Sujit Dey is an Associate Professor in the Electrical and Computer Engineering Department at the University of California, San Diego. Before joining UCSD in December 1997, he was a Senior Research Staff Member at the NEC C&C Research Laboratories, Princeton, NJ. He has been involved in the research and development of design methodologies and tools for low-power and high-performance VLSI systems, with particular focus on hardware-software embedded system-on-chips using nano-meter technologies. His research group at UCSD is currently working on developing adaptive protocols and flexible architectures for energy-aware mobile multi-media communications. He is a co-author of over 75 journal and conference papers, and 10 U.S. patents. He received Best Paper awards at the 31st and 36th Design Automation Conferences in 1994 and 1999, the 11th VLSI Design Conference in 1998, and several best paper nominations. He is a co-author of "High Level Power Analysis and Optimization" (Norwell, MA: Kluwer, 1997).

Dr. Dey is currently the General Chair of the 2000 IEEE International Test Synthesis Workshop, and the Vice-General Chair of the 2000 IEEE VLSI Test Symposium. He has also served on the program committees of several conferences, including the International Conference on Computer-Aided Design, the International Conference on Computer Design, the International Test Conference, and the VLSI Test Symposium.