First, background will be provided on embedded DRAM process, circuit and market issues. The term system-on-silicon has been used to denote the integration of random logic, processor cores, SRAMs, ROMs, and analog components on the same die. But up to recently, one major component had been missing: high-density DRAMs. Today’s technologies allow the integration of significant amounts of DRAM memory for applications such as data buffering, picture storage, and program/data storage. In quarter-micron technology, chips with up to 128 Mbit of DRAM and 500 k gates of logic are eminently feasible. This enlarges the system design space tremendously since system architects are no more restricted to standard commodity DRAMs. We will discuss the market for embedded DRAM applications as well as the associated challenges.

Second, we will describe the system design requirements for a typical application domain that can benefit from an embedded DRAM solution. The Hard Disk-Drive (HDD) controller application, which is a very typical application for an embedded DRAM solution, will be used as a vehicle to highlight design issues related to such systems-on-silicon design flow, required views, HW/SW-codesign, testing aspects).

Third, we will address issues in system design technology and compilation for embedded data-dominated multi-media applications. We will show that decisions made at this stage heavily influence the final outcome when the appropriate architectural issues of the embedded memories are correctly incorporated. Techniques addressed include formal data-flow analysis, reuse and access analysis, the most important memory related data-flow transformations and cache related allocation transformations, techniques for memory estimation, coarse-grain and fine-grain compiler transformations to improve locality, data partitioning and layout schemes, instruction selection and code compression.

Finally, we will discuss emerging CAD and synthesis techniques addressing the automatic incorporation of embedded memories into the design flow. Traditional behavioral and RT synthesis tools have relied on user hints and have viewed memories as a generic resource with a fixed (and simplistic) access protocol, leading to inefficient utilization of available architectural features. We will describe techniques to model a
variety of efficient access modes of modern memory families and algorithms for exploiting the architecture knowledge.

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