High-Performance and Low-Power Compiler Techniques for Parallel Embedded Systems

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Abstract

Multi-core SIMD processors and embedded processors with scratch-pad memory are considerably used in embedded systems. Data shifting operation takes much time when SIMD instructions are generated in multi-core SIMD processors. In this talk, we introduce some loop transformation techniques for reducing data shifting operations and for enhancing parallelism of outer loops for some real applications. For scratch-pad memory (SPM) architectures, we propose a compiler-assisted iteration-access-pattern-based space overlapping technique for dynamic SPM management with DMA (Direct Memory Access). Through this technique, we can exploit the chance to overlap SPM space to further utilize the limited SPM space and reduce the number of DMA operations. We also introduce a dynamic SPM management with data pipeline, in which we integrate group multi iterations into a block, and implement the block-level data pipeline between CPU-SPM and SPM-DMA. Therefore the serious overheads of the off-chip memory access by overlapping CPU execution and data transfer can be hidden. Finally, a dynamic voltage and frequency scaling for SPM-DMA based Embedded Systems is also introduced so that we can reduce the power usage by scaling down the supply voltage and frequency as much as possible.