Power-Aware Compiler Controllable Chip Multiprocessor

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Chip multi-processors (CMP) have attracted much attention since they achieve higher performance but not by raising operating frequency but by utilizing a number of transistors in parallel. However, simply increasing the number of processor elements (PE) will result in raising power consumption. This work presents a power-aware compiler controllable heterogeneous CMP and its performance and power evaluation with the OSCAR (Optimally SCheduled Advanced multiprocessorR) parallelizing compiler[1].

The proposed CMP supports multigrain parallel processing. It consists of multiple PEs, an interconnection network and a centralized shared memory (CSM) as shown in Figure 1. Each PE is equipped with processor cores, local memories, data transfer units (DTU) and power control registers (FVR) that change clock frequency and power supply voltage to functional blocks. The architecture maximizes performance by reducing execution overhead of parallelized tasks, such as memory access, synchronization and data transfer time as well as to reduce power consumption.

The OSCAR compiler realizes coarse-grain task parallelization of a program along with power reduction. It decomposes the program into macro tasks (MT) and generates a macro task graph that represents inter-task parallelism as shown in Figure 2(a). Then it schedules MTs onto PEs and apply the power saving scheme using the scheduling result as described in Figure 2(b). In the scheme, the compiler generates FVR set-up codes, such as power-off for PEs in idle, and clock / voltage change for PEs scheduled with tasks that have affordable time to be processed[2].

Performance is evaluated using the compiler and an architecture simulator of the proposed CMP as presented in Figure 3. MPEG-2 encoding on the proposed CMP with four homogeneous SPARC CPUs results in a 26.4 % power reduction while achieving 3.0 times speed-up against its sequential execution on one CPU. In addition, MP3 encoding on a heterogeneous CMP with four CPUs and four accelerators (Hitachi’s FE-GA) results in a 53.9 % power reduction at 21.1 times speed-up against its sequential execution.

References