Tutorial 3

Formal Verification of Digital Circuits
Ashraf Salem

Outline

For more than two decades formal verification of digital circuits is a hot research topic and in the last ten years this technology finds its way in the industry where EDA companies have produced a number of efficient tools. This tutorial covers the various techniques used to verify the correctness of combinational and sequential circuits. Also, the verification of properties using model checking will be discussed. The topics covered in the tutorial are: HDL based verification, Binary Decision Diagrams (BDD), SAT solvers, Theorem provers, Combinational Equivalence Checkers, Miter Circuit, SAT / BDD partitioning, Finite State Machine traversal algorithms, Model Checking.

Tutorial Presenter

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Ashraf Salem holds a Ph.D degree in Computer Engineering from Grenoble University, France. He developed one of the first VHDL based formal verification tool in the eighties. Prof. Salem is a senior engineering manager in Mentor Graphics Egypt; also he is a professor of Computer Engineering in Ain Shams University, Cairo, Egypt. He published over 40 articles in the fields of formal verification, semantics of hardware description languages and Hardware/ Software Co-Design.