Innovative Architecture for Future Generation High-Performance Processors and Systems
Innovative Architecture for Future
Generation High-Performance
Processors and Systems

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Preface

This edited volume collects papers, which resulted from presentations at the 2000/2001 International Workshop "Innovative Architecture for Future Generation High-Performance Processors and Systems". The meeting took place at the Maui High Performance Computing Center in January of 2001. A variety of topics in the areas of computer architecture, compilers, and applications were discussed. The workshop's special topic this year was power-aware memory hierarchy. As always, high-performance computing was also discussed. One of the workshop highlights was a presentation and discussion of the "Earth Simulator" supercomputer being constructed in Japan to study global change phenomena.

A total of 19 researchers from the US and Japan representing both academia and industry attended the workshop, presented their current work, and discussed future directions. A total of 12 presentations were made followed by extensive discussion. These were selected for the workshop based on refereed abstracts. The papers in this volume are extended from the work discussed at IWIA'01. They were selected by the program committee after additional refereeing. (Note that not all attendees chose to submit a full paper).

We thank all the participants and the program committee for an interesting and productive meeting. Dr. Robert Graybill of DARPA/ITO has been instrumental in his support of the workshop and its focus on power-aware computing. Our special thanks to the Maui High-Performance Computing Center, especially its director, Gene Bal, and Candace Shirley for their help and continuing support.

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