Plan Ahead for Yield

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1. Yield is important to everyone
As a system design house focusing on network products, Cisco is facing similar challenges as the industry in our silicon design practice. Time to market and quality of products are the two key drivers. To achieve our goal, our design practice is no longer limited to RTL design and GDSII tape-out. We are engaged in each stage of a silicon design and production cycle, from library selection, design implementation, production, test development and yield optimization.

Time to market has direct impact on the success of our products. A good silicon yield is critical for our production ramp up. More and more attention is given to the production cycle after tape-out. However, to achieve a good silicon yield, effort must be made even before the design starts. A good redundancy plan for yield improvement based on sufficient understanding of the yield model is critical. Contributions from everyone, foundry, library provider, test house and design team are necessary for design success which is important to everyone.

2. Memory yield is a primary factor for overall yield
Memories are denser than random logic and prone to defects and low yields. To improve memory yield, redundancy is usually used.

As commonly seen in networking silicon designs, our ASICs are memory intensive, as a result memory yield has become a primary factor for overall yield. To achieve a “reasonable” yield for our design, redundancy is necessary. It requires cooperation among all our partners: foundry, memory IP provider and test solution provider and design team to create a quality redundancy scheme.

3. Plan ahead and plan well
Understanding of the yield model is critical. We need to understand the difference between logic yield and memory yield and the impact of different redundancy and repair schemes on memory yield. An efficient redundancy scheme for memory can reduce the impact in terms of area overhead and routing congestion and achieve high yield improvement.

Testing and debugging memory failures on the tester and in the system demand a good test and debug scheme. Different memory cell designs are prone to different types of defects. A good test solution should adequately address this issue. Repair is tied closely with how the memory is tested and a good repair scheme provides testing and repair of memory at different production stages. Very often during the initial device bring up stage, an unexpected hazard can cause test fluctuation. A good debug scheme can ensure a good data collection and analysis process.

To achieve good memory yield, plan ahead and plan well. The following is a list of items needed through planning before design tape-out:

- Redundancy and repair scheme
- Debug scheme
- Design implementation
- Test and repair on the tester
- Data collection

4. Communication
Communication is a key to achieve a successful partnership. All parties involved have different expertise. It is important to share the expertise to achieve understanding at an early design stage, and to build on the expertise to achieve an efficient yield plan.