At Intel we are very focused on the Cost of Test, but we try to keep it in the proper context and focus on the Cost of Quality. By working with our customers, our Quality & Reliability group establishes required quality metrics for our products and the process steps to monitor outgoing quality. The quality goals are used to drive the test process as a whole and we optimize the steps within the process to minimize cost to Intel. For example, we optimize the content at wafer sort to achieve cost effective packaging yields (note this is NOT ppm level screening), provide feedback to the fab, and provide information to allow process optimization post packaging (for example, optimizing Burn-In). We start with fairly exhaustive flows and content and then quickly minimize them based on manufacturing data (like eliminating extra test sockets, conditions or non-effective or redundant patterns).

Because we have very aggressively pushed our silicon processes and have narrow speed bins, we have seen a limited increase in the test issues as we have progressed down to 90 nm processes. As the maximum Vdd has scaled down, there has been a shrinking of the operating Vdd window, which aging has further degraded. This has significantly impacted if not eliminated some of the low Vdd test methods and resulted in new features that have their own test challenges. I am predicting these effects will result in increased cold temperature sensitivity which will further impact our test flows.

DFT has been key in our efforts to manage test costs while meeting our quality goals. Our HVM products have focused DFT to enable tester reuse or to enable low capability testers (ref Realizing the Benefits of Structural Test for Intel Microprocessors M. Mayberry*, J. Johnson, N. Shahriari, M. Tripp, Proc ITC 2002 pg 456). While we continue to rely more on DFT supported test methods, we see no path to eliminating functional testing (FT) on CPU’s, complex chipsets and communication products. We have tools to guide FT development and continue to focus on minimizing the functional test generation effort (ref FRITS—A Microprocessor Functional BIST Method P. Parvathala*, K. Maneparambil, W. Lindsay, Proc 2002 ITC pg 590). The test cost optimization efforts are limited by what has a positive Return on Investment (ROI), meaning we need to get more in product savings than we will spend to gather the required information and implement the changes. On low volume products this generally means we will only do socket level optimization; for high volume products, we will pursue opportunities to reduce test time by 100’s of mili-seconds. We continue to pursue generating content for advanced fault models (n-detect, bridge, transition faults, ... ref 2004 DBT Workshop Keynote address) which drives up test data volume and test time and I continue to be an advocate for DFT to enable data compression techniques that also minimize the test application time.

Top Things to Manage Cost of Test

1) Have Manufacturing Feedback systems that enables Fab and Design to address root causes for “Likely” or hard to screen failure modes. There is no substitute for a clean fab process and robust product design. Establish DFM requirements/goals during product definition and design.

2) Standardize the test interface where reasonable. This has enabled tester reuse and leveraging Moore’s law to enable development of lower cost equipment.

3) Establish Test Cost goals during product definition and develop and use predictive models for test content and test time. Recognizing a problem is the first step in solving it. Also, continuously monitor progress against goals and use current data to establish goals for the next product.

4) Globally optimize over the entire test process, do not locally optimize one step at the expense of another. This includes utilizing DFT. Understand the product area and design cost vs the benefit (although realize that during the design the cost will be more clear than the benefit and DFT often benefits debug and process learning). Always look for DFT that enables the test problem to be avoided completely.