Panel 7 : Cost of Test – Taking Control

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Summary: Nanometer technology have not only resulted in increasingly complex chips but is also exposing new defects and failure mechanisms during manufacturing that are challenging process and test engineers while they struggle to maintain high yield and low DPM. Silicon manufacturers are increasingly using structural test vectors to improve the process and consequently, reduce the defect rates. Structural vectors help detect defective parts and debug issues in an automated manner, which subsequently allows ramping up the yield for a given process fairly quickly. In addition, it reduces the number of escaped parts thereby guaranteeing lower DPM and fewer field returns. However, relying more on structural tests implies that the test set should be of the highest quality and may include vectors for fault models (in addition to stuck-at faults) such as transition, path-delay, bridging, n-detect, in-line resistance, Iddq, etc., covering some of the new failure mechanisms.

As test engineers are looking towards more test vectors to lower the DPM, the manufacturing test cost is fast rising. The rise in test cost can be attributed towards increasing device complexity as well as higher number of test vectors required to obtain a good quality test set. For example, the number of test vectors targeted for at-speed fault models are usually 3-5X more than stuck-at fault patterns. As vectors for n-detect and bridging faults are added, the test set size can grow even further. The number of test vectors affects test cost directly as it increases test data volume as well as scan test application time. Test data volume translates into the need for added tester capacity or need for tester re-loads that indirectly increase test time. Whereas, test application time reduces tester throughput as the total test time per device increases.

With such rapid increase in manufacturing test costs, companies are searching for new ways to control, and in many cases, reduce the costs associated with test. There is a constant strive to achieve a balance between test quality and test cost, and since test quality is non-negotiable, the challenge is to contain test cost by guaranteeing the highest test quality. The motivation of this panel is to invite experts representing different segments of the semiconductor industry, and listen to their experience regarding the factors contributing to cost of test and learn some of the techniques they have been adopting or suggesting to their customers to contain cost of test. Specifically, some of the issues that will be discussed are as follows.

- What are the major contributors to cost of test? What are the design characteristics that are responsible for increasing cost of test?
- Rising manufacturing test cost – is it hype or reality? How big an issue it is in various segments of the semiconductor industry?
- What are the major drivers of ATE cost? How can some of the ATE features be exploited to reduce cost of test?
- How does one optimize between rising test cost and stringent quality requirements? How much testing is enough?
- What are some of the possible solutions in order to contain the cost of test?
  - Embedded compression
  - Pseudo-random logic BIST
  - Multi-site testing
  - Low cost DFT ATE
  - Analog BIST
- What are the advantages and disadvantages of various approaches currently available?

Finally, the panel will address some of the upcoming technologies in the horizon that would further push the envelope of requirements for manufacturing test thereby continuously challenging current methods employed to contain/reduce cost of test.