What Do You Mean My Board Test Stinks!

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For years at ITC we have debating about how to measure ASIC coverage. Over the years, though, we have never talked about measuring test coverage at the board or system level. As difficult as it is to get consensus about ASIC test coverage metrics, it is magnitudes more difficult to come up with a way to measure coverage at the board level. Board level testing must not only account for the functionality and performance of all the devices placed on the board, but it must also account for how the devices are assembled on to the board and how the devices interact with one another. Because of this level of complexity, the industry has avoided trying to come up with a “comprehensive” test coverage metric which accounts for all possible defects which may occur at a board or system level. Instead the industry has focused primarily on the assembly portion and “assumed” that the devices placed on the board were “known good”. Even limiting the scope to assembly process, there is still a great deal of controversy in finding a metric to determine how well the product has been assembled.

There are three general areas of board and system level testing: structural testing, functional testing and parametric testing. Software testing may be a consideration but is out of the scope of this panel. Structural testing focuses on the assembly process described above. There are aspects of structural test that can be easily described in terms of coverage: shorts, opens, stuck high, stuck low. Other aspects such as the quality of the solder joints may be open to some interpretation. Parametric tests also have well defined metrics: bit error rate, and jitter for example. However, these metrics are much more difficult to tie to actual defects. Functional testing is the least well defined of the three test areas. There are no metrics used to determine the effectiveness of the functional test. Rarely is there much thought given to what types of defects the functional tests should be targeted. Instead, coverage is generally a consequence of the functional test. Coverage analysis for functional tests is still, in many cases, an ad-hoc process.

The panel will take two sides of the problem and then try to work inward. First, the panel first will try to determine if it is possible to define a test coverage metric or methodology which comprises all possible faults/defects that may occur (both at the device level and at the board/system level). The panelists will consider the different aspects related to coverage including assembly and process related defects, component defects and component interaction defects. The panelists will also discuss the capabilities of various test methodologies and techniques to detect defects/faults, whether or not it is feasible to assign fault metrics to those test methodologies/techniques and if so, what kind of metrics should be assigned to the various test types.

Ultimately, the goal of the panel is to determine if there is a consistent way to measure the ability of a board to perform as specified in the system (i.e. my board test doesn’t stink after all). Given the complexity of this problem and the number of different board and system level test techniques, there should be plenty of discussion on how best to tackle this problem.