Test Strategies for Nanometer Technologies

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The Growing DPM Challenge

The trend toward bigger systems-on-a-chip means that the increase in die size alone will add significant DPM, making the goal of double-digit DPM using current methods infeasible. But feature scaling continues to double device counts with every process generation, at the cost of new, more subtle defects. Decreasing threshold voltage increases noise susceptibility noise. Thinner, taller wires dominate propagation delays, and are more vulnerable to cross-talk. In-die variation exacerbates marginalities. To keep quality under control in nanometer processes, test must directly target delay defects, noise and process variation.

The Role of Functional Test

Functional testing of high-performance parts continues to screen significant unique DPM on top of high coverage scan content. But functional test generation has largely been an expensive manual process, and comes at high time-to-quality and test application costs. Where the design architecture is amenable, it will make sense to automate functional test generation, particularly if on-chip resources can apply the content and accumulate results.

Automation of functional test generation in the general case is likely to remain intractable and we must look for ways to capture its benefits using structural means. The primary benefits of functional testing appear to be:

• At-speed testing in native mode.
• Better coverage of relevant marginalities
• Coverage of areas not covered by DFT.

At-Speed Structural Test

Structural delay testing has been slow in making it out of the research domain into high-volume manufacturing. While transition fault testing has been used with some success now, the tests are usually run conservatively at a slower-than-functional speed. The concern is that at-speed tests could result in heavy yield losses because they are applied in non-native mode, and could target functionally unsensitizable paths. Getting the most out of delay test will require close integration with timing analysis (to select low-slack paths), and with formal verification (to avoid over-testing). In addition, DFT must support reliable at-speed test application methods.

Defect-based Testing

With the proliferation of subtle defect types in nanometer processes, targeting defects directly is essential to containing test data volume. To this end we need tools that can be used to identify configurations susceptible to defects or marginalities, and to create test content to target them. This strategy necessitates a tight feedback loop between manufacturing and test, including monitoring and characterization of failure mechanisms, and adaptation of test content to keep it relevant. Early in the life of a process technology, the feedback learning will translate to time-to-quality costs. The alternative to targeting defects is to use stochastic approaches such as N-detect and BIST, which are not dependent on feedback from manufacturing. But N-detect content tends to be O(N) in size, and a 5-detect test suite that includes stuck-at and transition faults could be prohibitive. Without a feedback mechanism, response to DPM excursions would be limited.

Comprehensive Coverage

Test generation for large SoC designs is approached on a partitioned basis. IP cores and arrays are treated as black boxes, and large logic units are partitioned to make them ATPG-friendly. This approach often leaves many boundaries that are inadequately tested. For example, a multi-port memory might only be tested through one port, and partition boundaries may be held constant during test generation. High-speed I/O’s, which increasingly contain analog circuits, might not be tested well using a structural approach. A comprehensive structural test strategy needs a detailed plan to cover all the boundaries, at speed, including testing for marginalities.

What Price Quality?

Recent developments in test compression have opened the door to richer structural test content. Creating that content will require a closer integration of design, test generation, and manufacturing. However, each promising test method has associated costs. The question of whether we can achieve double-digit DPM must be accompanied by the question: can we afford it?