Achieving 100 DPPM on today’s complex ASICs is a realistic but difficult proposition. More importantly, with the current state of the art testing, it remains a very costly task that often times takes many months of DPPM reduction efforts in manufacturing to achieve due to a reliance on functional or system level tests. The challenge is not whether 100 DPPM can be achieved, it can. The real challenges are being able to deliver this quality level from the first prototype lot, not impacting the design cycle time and minimizing test cost such that profit margins can still be met. The following sections describe what this author believes are the key ingredients in achieving 100 DPPM without functional testing and the advances that are needed to meet these challenges.

**Structural testing**

Certainly the cornerstone corner stone to achieving 100 DPPM or even reasonable quality levels is a well planned structural based test strategy. In today’s complex ASICs, where internal gate to IO ratios are exceeding 10,000:1, it is no longer possible to obtain the required test coverage without proper design-for-test (DFT) and scan based testing. Historically, the measuring stick for DFT was the stuck-at fault (SAF) test coverage a design could obtain with scan based test. However, very deep submicron (VDSM) and nanometric designs require additional structural testing such as transition delay fault (TDF) testing. This requirement places additional constraints on the DFT. For example, when employing a launch-off-shift TDF pattern architecture, the scan chain order can play a significant role on the obtainable coverage.

Achieving 100 DPPM with structural testing requires nearly perfect SAF and TDF coverage, but this alone is not sufficient. There are a large number of defects that cannot be adequately described by either fault model, but which are often times fortuitously detected by these patterns. Node-to-node bridging defects and stuck-open defects can manifest themselves as logical faults that require more complex excitation and observation conditions. The exact behavior and detection criteria depend on the layout of the device as well as the location and physical properties of the defect. Statistical methods based on simple fault models have been developed and proposed that increase the probability of detecting these types of defects because current ATPG tools have no knowledge of the layout. N-detect testing for example, redundantly detects stuck-at faults multiple times and has shown to detect a significant number of defects not detected by traditional SAF patterns. Along with the increased probability of detection comes the cost of a rapid increase in test data volume and an increased number of test vectors that do not provide any additional benefit. Additionally, this shotgun approach does not give any preference to and cannot ensure detection of those defect sites that are more likely to occur. Layout based defect site extraction and deterministic ATPG on the other hand can minimize test data volume and provide coverage where it is most needed, but the complexity of the ATPG problem will drive longer cycle times in pattern generation.

The bottom line is that to ensure a repeatable and cost effective realization of 100 DPPM with structural based test, a mixture of deterministic and statistical or pseudorandom patterns will be required. Many advances are needed in the ATPG process to include layout and timing knowledge for proper deterministic pattern generation. In addition, to keep test costs manageable, built in self test for the logic will be required to apply a massive amount of pseudorandom vectors with short test times and without requiring costly ATE resources.

**Outlier screening and defect based test**

Defect based test methods that focus on outlier identification and removal from test data sets such as IDDQ, Fmax and MinVDD are a critical component in achieving 100 DPPM. The exact contribution to the DPPM of not performing these tests varies over time, but can be on the order of 200 - 400 DPPM from a typical mature baseline defect distribution. While it is needed, replacing go no-go testing with binary timing or voltage searches can increase test costs by a factor of 5-10 times. Methods such as reduced vector set feed forward testing and statistical post processing can dramatically reduce this cost [1]. Continued advancement in defect based test will be critical to reducing test cost associated with it and in maintaining the effectiveness of these screens (for example, maintaining IDDQ based test effectiveness in the face of increased leakage current in nanometer technology).

**Adaptive test**

Today, test cost (in design and manufacturing) is the biggest obstacle in achieving 100 DPPM. Adding all the additional tests can easily inflate test costs by an order of magnitude. Although all these tests will eventually be necessary, the defect distribution will change significantly over the lifetime of a device and at any snapshot in time the required testing will only be a fraction of the entire test suite. It is therefore necessary to have a test strategy that allows the test program to evolve over time and adapt to the actual defect distribution. This will not only reduce test cost but, by being able to proliferate additional test vectors when necessary, adaptive testing will help ensure consistent quality and reliability results over the lifetime of the device. While adaptive test is in its infancy and only conceptual, there is evidence that suggests it can have a significant impact in reducing test cost and improving quality [2].

In conclusion, 100 DPPM is possible today and will be achievable in nano-technologies, but the challenges outlined in this paper will need to be addressed in order to achieve this goal consistently and in a cost effective manner.

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