Test AC-coupled digital pins with 1149.1 and 1149.4

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It has been recently proposed that an “AC-EXTEST” extension to 1149.1 be created to address testing of capacitor-coupled digital pin signals that cannot be tested by a low speed 1149.1 EXTEST sequence.

One proposed criterion for the AC-EXTEST proposals is that TCK is allowed to be a free running, low frequency clock that can pause anytime, so that all existing board testers remain usable. That was important when all digital faults were stuck-ats, and the technology for delivering patterns at 1 Mb/s was just emerging. But presently, timing-related defects are of greater concern, and sustained TCK frequencies up to 10 MHz are quite practical. It may be more important that board designers are able to use existing ICs, and chip designers are able to use existing boundary scan cells – it is likely easier to get a tester that can produce a known TCK frequency, with predictable pauses, especially since a faster TCK decreases total test time. A predictable time interval between an update and a capture can be very useful.

The range of capacitances that must be tolerated is limitless in theory, but in practice a 10 nF capacitor provides better coupling than a 10 pF capacitor, it costs about the same, and it requires about the same board area. For a 50 Ω resistance and 10 nF capacitance, the time constant is 500 ns, which allows enough time for a 5 MHz TCK to update a register and capture the received value before the voltage has decayed too much. By waiting additional Run-test/Idle cycles before a capture, one can test that after sufficient time has elapsed, the signal voltage has indeed decayed completely. With a known voltage threshold, the RC time constant also can be tested this way [1].

All the proposals use receivers that monitor the differential signal pairs as two single-ended signals, which means they are sensitive to noise. Noise can easily make single-ended receivers useless (though using Schmitt-trigger inputs helps), hence the need for differential receivers in the first place. Therefore, an AC-EXTTEST must be able to assume that signals can be controlled (and are hence silent) or are sufficiently isolated to cause only low level noise during testing.

There are paradoxes here. To make a digital approach work, it needs to be noise insensitive when monitoring each signal of a differential pair, yet a differential pair is only used when a single-ended approach is too noise-sensitive. Employing a noise tolerant test on each single-ended signal will fail to detect some faults, because noise is a key source of faults. An analog approach is needed to resolve these paradoxes, and 1149.4, being the analog extension to 1149.1, is a candidate approach.

For some circuits, it is important that the capacitance and termination resistance are individually measured. For these cases, 1149.4 is likely the best, if not the only, standardized solution. This approach allows a complete structural test that is independent of voltage levels and switching points. In terms of performance degradation, the impact of the circuitry that 1149.4 requires for a differential receiver is comparable to that in the proposed digital-only solutions. Some people regard 1149.4 as too slow because it requires sequential testing of pins, and if there are thousands of such pins, the test time becomes prohibitive. This argument assumes conventional test approaches – novel approaches are possible, and more will evolve, to greatly accelerate this test time. A better argument is that 1149.4 is not yet widely known or usable because it is so new. This chicken-and-egg problem can only be resolved by market demand, and by manufacturers supplying 1149.4 ICs ahead of that demand [2].

To conclude, existing 1149.1 can be used in many cases, with a suitable TCK frequency to test AC-coupled signal lines for a practical range of capacitance values. For some circuits, where the exact termination resistance is important, or where there is a lot of high frequency noise, only 1149.4 offers a thorough test.