Learning to Knit SOCs Profitably
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In the broadest sense, a System-on-Chip (SOC) is a semiconductor product that incorporates significant circuit blocks (cores) from more than a single design group. Along this definition, every semiconductor manufacturer who has ever reused a large circuit design within a larger product has created a SOC, as has every ASIC designer who has ever used a foundry's memory arrays or large-scale library circuits.

Despite this potentially broad meaning, intense interest in SOCs is widespread in the semiconductor industry, and this interest is energized by a narrower definition. Specifically, the potential for a semiconductor product to be created by a first design group by incorporating significant circuit blocks from a second, a third, and possibly further design groups represents a significant step in the industry’s maturation. This definition of SOC is exciting because such a SOC promises to enable a greater degree of specialization, and therefore semiconductor industry efficiency. New efficiencies enable new value creation. Specifically, designers with the capability to define important circuits can leverage their expertise as core providers in a broad market, while entrepreneurial system integrators with the insight to accurately predict emerging functional requirements are able rapidly to create low-cost high-performance products. Under this scenario, the future would witness a rapid proliferation of SOCs of high complexity yet with short intervals from concept to first revenue.

Is this bold vision of SOC-enabled semiconductor industry growth really feasible? The fundamental design and test challenges for SOCs are increasingly well understood. However, a formidable economic obstacle to SOCs is born of well-established semiconductor manufacturing practice. Current and foreseeable methods of making chips require that a single manufacturing process create the active circuit elements. Semiconductor manufacturers rely on an ability to tune their manufacturing processes to facilitate achieving product goals. When it comes to combining two or more specialists' circuits in a single semiconductor product, whose specialized process will be used? Which core provider will make critical design and process information available to another manufacturer for purposes of SOC integration, and thereby expose the intellectual property on which his existing business is based? If most companies are unprepared to place their precious intellectual property at risk, then the nascent SOC industry could be relegated to a more modest future wherein cores represent merely one, possibly convenient way for an ASIC designer to implement moderate-performance functions.

The challenge before those responsible for testing SOCs is to anticipate the resolution of such business issues, and to address the significant technical issues that arise. Test industry experts have begun to explore the many facets of effective testing of SOCs. Because of the subtle ways in which circuits interact to promote (or in some cases frustrate) testability, enormous complexities surround the question of how to develop high-quality tests for SOCs in short periods of time. It is well known that manufacturing a new high-performance semiconductor product requires close interaction among test engineers, design engineers, and process engineers. The same pressures that tend to make semiconductor manufacturers leery of the SOC business model would also tend to create significant organizational and communication barriers to rapid manufacturing ramp of SOCs.

General solutions for SOC test appear to demand new models of partnership among core designers, system integrators, test system manufacturers, test engineers, and process engineers. Each of these partners possesses unique value to contribute to the fundamental understandings that will enable the successful management of the interactions among disparate circuits. Progress towards this goal of cooperation is hastened to the extent that the partners adopt standard practices, which trade off small restrictions in flexibility against large decreases in time to revenue through test.

The opportunity before our industry is to identify conditions that allow reasonable semiconductor product performance while also providing a degree of regularity that is sufficient for EDA tools to achieve the required testability. However, the EDA vendors cannot be expected to figure out solutions to all of the problems; they need help from the rest of the industry. Well-supported standards activities provide a means for gleaning lessons from the pioneering visionaries who lead the industry. The potential rewards for those who teach themselves and their partners how to achieve the boldest vision of SOC are tremendous.