Spice up your Life : Simulate Mixed-Signal ICs!

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Philips Semiconductor is a supplier to a wide range of markets for analogue and mixed-signal consumer ICs. These products extend from the simplest form of linear products to advanced VLSI analogue systems such as the One-Chip TV. For new mixed-signal products Philips has started to adopt a strategy of testing similar to that used for digital ICs. This is based on efficiently proving the product is free of known defects or other process deformations. This is referred to as DOT or Defect Oriented Testing. It is an alternative to testing the device in production purely to its specification, this has more recently been called SPOT, Sspecification Oriented Testing. SPOT is used within Philips but preferable only for device verification and validation as part of design or early in the Test and Product Engineering (TPE) cycle.

DOT testing as a formal method emerged within Philips in the mid-1980s, as part of an earlier Anglo-French trend, initiated by the Esprit CATE Project, towards a Divide and Conquer based digital IC testing strategy. Within Philips this is referred to as Macro-Test, which has been unified within Philips into a company wide design and test flow. A basic theory for Macro-test and DOT was given by CMU in the seminal work on the causes of Yield loss by CMU in the 1980s. In this theory the need to screen a product for yield loss is developed as part of a unified approach to product quality assurance. Nevertheless the application of this approach to analogue ICs would have to wait another five years, until conservative objections to a full DOT approach could be disproved by the Esprit project Artemis. Essential to this breakthrough within Philips was the realisation that in many product areas, defects are fundamentally more harmful to the quality image and reliability of a product, than “softer” specification issues. For customer quality perception, a demonstrably mal-functioning product, is at least an order of magnitude more harmful to the image of quality than a fuzzy missed specification. Maybe this is specific to consumer products? Our belief is that this is not the case, and in any application, a defect, though minor, is always a greater threat to reliability. Specifications are assured by analogue design, i.e. matching, which are bound to relative not absolute parameters of the process. Such process deviations are a lesser threat to reliability.

Defects are fundamentally more harmful to the reliability of the product because they lead to electrically deviant flows of current and incorrect biasing of internal circuitry, which can degrade both the long and short term reliability of the circuit, e.g. hot-electron degradation. This is generally not true of specification weaknesses. Moreover, defects are electrically unreliable. All major classes of CMOS defects: opens, interconnect shorts and gate oxide short originate in deformation of oxides and conductors, a significant minority of such defects are unstable oxides that can vary in resistance over time or temperature. If this resistance should fall below the critical resistance of the fault the circuit will start to exhibit functional problems, that will accelerate over time as the oxide degrades i.e. TDDB, Time Dependent Dielectric Breakdown. For safety critical applications it is argued that some form of fault model is essential to ensure reliability at reasonable cost.

A Philips’ paper “Defect-Oriented Testing of Mixed Signal ICs: Some Industrial Experience” by Y. Xing in the ITC98 proceedings gives a refreshing new viewpoint on mixed-signal testing of automotive ICs. It provides clear examples of the advantages of introducing DOT, with a defined fault coverage metric. Taking the second example of the paper, an automotive IC used as a child safety controlled air-bag trigger, the need for high fault coverage is clear to everybody. However, this approach to MS IC testing which merged the best in class digital and MS test methods shows that analogue fault simulation has other advantages. In terms of

- Test time
- Test development effort
- TTM
- Diagnosis

The message is clear when using a fault coverage metric for mixed-signal test development the advantages of digital testing appear. Experience from large ICs such as the One-chip TV shows that such techniques also allow innovative DfT schemes to be devised that directly attack the issues of mixed-signal testing by divide and conquer, e.g. the ICCQ test method. Such methods are not compatible with SPOT. Spice up your life, fault-simulate those mixed-signal ICs!

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