Core reuse is an emerging IC design style which enables rapid development of highly complex ICs. Reusable circuit cores come in two basic varieties, hard and soft. Hard cores are optimized for area and performance and are not modifiable by the user, whereas soft cores are user modifiable. If soft cores do not contain testability (i.e. scan/BIST), it can be inserted into the core by the user. Hard cores cannot have test features inserted by the user. Hard core providers should therefore include some means of testing the cores to prevent users from having to add testability external to the core, using pin access or scan/BIST collaring for example.

In addition to the hard and soft core varieties, cores will be available for reuse with and without IEEE 1149.1 test access ports (TAPS). Non-TAP’d cores are circuits that don’t have the need for a TAP architecture. They may be scan or BIST testable via a simple, instruction-less test interface. Testable, non-TAP’d cores could be viewed as 1149.1 test data registers that simply plug into an IC’s boundary scan TAP domain to be accessed by TAP instructions.

TAP’d cores are circuits that demand the need for a TAP architecture. One thing that will help the testing of TAP’d cores is the fact that most of these cores will have evolved from a previous life as an IC. Such cores will typically maintain the IC’s TAP architecture and instruction based testability features. These testability features will be just as useful inside an IC as they were on a board, especially interconnect testing if cores maintain a boundary scan test capability.

One reason why TAPs will be maintained during the migration of a design from IC to core form is that the TAP provides access to features other than boundary scan. For example, many producers of DSP and CPU ICs take advantage of the TAP’s instructioning capability to regulate access of internal scan BIST, and in circuit emulation resources. Removing the TAP during the IC to core migration process would cripple access to these features and, in some cases, require a significant redesign. Such redesign would take time and would prevent reuse of the IC’s test and emulation schemes at the core level.

While TAP’d cores will not be the dominant core type, they will exist and must be anticipated by core users. IC providers will face a dilemma when ICs contain two or more TAP domains. That being, how do multiple TAPS plug and play together in a single IC? One option is to simply connect multiple TAPS together to form a serial TAP string. However, this option is not compliant to 1149.1, since 1149.1 does not allow TAP strings within ICs. Changing 1149.1 is a possibility, but the long range effect of such a change would be negative since it would spawn ICs with TAP strings. Each of these ICs will eventually evolve into cores with TAP strings. Over time, this IC to core evolution would lead to ICs that contain an unacceptable number of TAPS in one string.

Another option is to design ICs to where TAP domains are hierarchically selectable for test access. This option appears to provide a more solid framework on which to build a long term core reuse test technology. This option would be based on three key requirements. (1) Insure IC powers up with only the boundary scan TAP connected to the test pins. This maintains compliance with and simplicity of 1149.1 at the board and system levels. (2) Allow for any number or combination of TAPS to be concatenated with or substituted for the boundary scan TAP. This provides flexibility in optimizing core test access and control. (3) Insure 1149.1 scan control is used for TAP selection. This maintains a common thread of test communication and control at all circuit levels (i.e. core, IC, board, box, and system).