Embedded Core Test Plug-n-Play: Is it Achievable?

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The testing of embedded cores (or Virtual Components [VCs], as the VSI Alliance calls them) in an environment where the system-chip is composed of multiple cores from different authors, requires that the chosen test strategy and methodology allow for the identification of the failing core (VC), as well as determining that the manufactured chip is of sufficient quality to ship to a customer. This imposes several unique requirements:

**Test Access** – Need to provide access to the embedded cores from the primary I/Os.

**Test Isolation** – Need to isolate one or more cores from the rest of the system-chip for test purposes.

**Interconnect Test** – Need to test the connections between the cores. This may be “pure” wiring or include logic inserted by the system-chip designer (e.g. buffers).

**Shadow Logic Test** – Need to test the logic which lies in the “shadow” of the cores. Shadow logic is defined as logic that is accessible only from core I/Os, as opposed to primary I/Os. This logic may be user defined logic (UDL), an internal system-chip bus, etc.

Plug-n-Play is the ability to take the tests created for the individual cores, interconnections and shadow logic, and to integrate them into a single efficient test program. There are many test methodologies in use today that provide the required access, isolation and tests needed, such as, scan, core-boundary scan, BIST, $I_{DDQ}$ and test access multiplexers, to name a few. Unfortunately these techniques have a large number of variants which are incompatible with each other when placed on the same system-chip.

For instance, if scan is one of the chosen methodologies, one finds that there are many different scan latch implementations in use today. Some use master-slave configurations, some are level-sensitive as opposed to edge-sensitive, etc. Furthermore, the scan chain may be on dedicated core I/Os if it is a new core design, or if the scan was added during logic synthesis. It may be accessible through a special test mode if the core is a recycled design that used to be a stand-alone chip.

The activation and readback of BIST logic is another area where incompatibilities can be found.

$I_{DDQ}$ testing at the core level will require either dedicated power pins for the cores using it, or that all cores in the system-chip include a stand-by low current draw mode.

In order for Plug-n-Play to become a reality, the number and types of variants used by each of the test methodologies, will have to be narrowed down to a very few compatible implementations. The core designers and the system-chip integrators will have to adhere to these conventions (nee standards) in order to assure that their cores are mergeable, for test purposes, into a system-chip. These standards are being worked on today, under the auspices of the IEEE P1500 Embedded Core Test Group and the VSI Alliance Manufacturing Related Test Design Working Group. Only when these standards become available and designers start using them will Plug-n-Play become real.

**Conclusions**

Is Plug-n-Play achievable? Yes!

Is it Sufficient? Ahh there is the rub.

All of the above test methodologies are designed around detecting structural faults. Devices unfortunately suffer from manufacturing defects and not all the possible defects can be mapped into fault models. Resistive via plugs, coupling through the metal interconnects, out of tolerance $V_T$, etc., can result in defects that affect the device’s intended function, but which may not be caught by any structural test.

Evidence of this phenomena was presented by Sematech at the VLSI Test Symposium this year. The results showed that there are many defect types which have no equivalent faults models. The only way to observe the presence of these manufactured defects is through system-level functional tests, with guardbands on the power supplies and timing. Only in this manner will most of the latent defects that cause interaction problems between cores be observed and caught before customer shipment.