WHY WOULD AN ASIC FOUNDRY ACCEPT ANYTHING LESS THAN FULL SCAN?

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Abstract

A key force behind IBM’s growth in the application-specific integrated circuit (ASIC) market is the ability to sign off on multi-million-gate designs without requiring test vectors, presenting a savings in both time and money to customers. Once a customer ensures (via formal verification and/or functional simulation) that the design functions as required, static timing analysis (STA) ensures that the design achieves the required performance targets. Extensive model-to-hardware correlation assures correctness of the timing analysis models, enabling IBM to assure that the design can be manufactured to the required performance targets. Through a combination of full-scan and boundary-scan design-for-test (DFT) structures, the IBM ASIC methodology ensures that automatically generated test patterns will run correctly on test equipment; typically achieving 99+% stuck-fault coverage. In the case of a repeatable manufacturing defect, full-scan-based diagnostic software isolates the problem without customer involvement.

Partial-Scan vs. Full-Scan

Because one of the primary business goals of ASIC customers is a short “time to market,” IBM strives to turn around the layout, test pattern generation, and fabrication processes as fast as possible. STA and full-scan test structure verification (TSV) techniques are efficient and thorough methods of ensuring the successful manufacture of an ASIC to the customer’s performance specification. Any evaluation of which flip-flops or latches to leave out of scan chains, along with any resulting increase in test generation complexity, adds delay to the customer’s product schedule. Although sequential test pattern generation capability is required even for full-scan designs (e.g. for generating tests of certain clock-gating structures), the majority of tests are generated efficiently using combinational techniques.

Although a non-scan flip-flop or latch might be slightly smaller and have a slightly faster setup time than its scan equivalent, any potential advantages of partial-scan design must be carefully considered in view of the alternatives. Setup-time differences between scan and non-scan cells are negligible compared to the unpredictability of wire delays prior to layout. After layout, when wire delays are predictable, any benefit to be gained by substituting non-scan cells for scan cells must be weighed against possible delays in market entry due to design iteration and against any possible increase in manufacturing test cost. Furthermore, a technique such as cycle borrowing, which can remove the impact of setup time on cycle time, may prove to be more cost-effective than partial-scan design.

In addition to the time-to-market advantage seen by ASIC customers, full scan provides the foundation upon which several additional DFT features have been built:

- Full scan can provide the basis for debug of early hardware and/or software.
- Full scan provides access to built-in self-test (BIST) structures in embedded macros.
- Boundary-scan structures, incorporated into full-scan designs, allow thorough, yet economical, test of very-high-pin-count ASICs by connecting only a subset of pins to high-speed tester channels.
- Data compaction techniques, such as weighted random pattern (WRP) test generation and signature compaction, which typically reduce test data storage requirements by two orders of magnitude, are easily applied to full-scan designs.
- Full-scan-based diagnostic software assists in isolating repeatable manufacturing defects without customer involvement.
- Level-sensitive scan design (LSSD) is a full-scan design technique that enables the detection of manufacturing defects without impact from “design defects” such as performance-marginal design. Furthermore, LSSD enables a timed (ac) launch-capture test within a single tester cycle, providing “at-speed” test capability on test equipment that is incapable of operating at target application frequencies.
- Our experience has shown that full scan is instrumental in enabling reuse of cores. The small investment in design effort to implement full scan is returned in test bring-up savings after only a small number of usages of the core.

In conclusion, then, one wonders why an ASIC foundry would accept anything less than full scan.