Innovative Design Platforms for Reliable SoCs in Advanced Nanometer Technologies

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Abstract — An increasing demand for higher performance, lower power density, and greatly expanded functionalities will determine radical changes in the future computing architectures. These widely acknowledged emerging trends are however insufficient to address all the challenges introduced by advanced silicon nanometer technologies. It is well known that manufacturability for high yield, along with design productivity and predictability are major problems in gigascale System-on-Chip (SoC) design. Moreover, as technology advances deeper into the nanometer regime, a tight control on process parameters is increasingly difficult. As a consequence, variability will be a dominant factor in the design of complex ICs that must be addressed at the technology, circuit, and architecture level. In this talk, we will discuss the impact of systematic and random variations, and we will present a new architecture-to-silicon design platform based on the concept of regularity at different levels of abstraction. Moreover, we will also introduce an innovative design methodology to synthesize clockless circuits, which can be exploited to implement logic blocks that operate under process, power supply, and temperature variations.

I. INTRODUCTION AND MOTIVATION

The microprocessor that has sustained the Moore’s Law and pushed the technology scaling into the nanometer regime, and more in general computing architectures based on the microprocessor, are perhaps undergoing the most significant transformations since their introduction. To achieve the predictions of Moore’s Law, increased transistor density is of course important, but the next key challenge is to integrate the basic foundations such as process technology with system architecture, to drastically reduce the development cycle and NRE costs, to meet tighter time-to-market windows, and to achieve high yield to compensate for the soaring economic investments necessary to develop the next nanometer technology nodes and build the manufacturing facilities. Such trend will dictate a deep rethinking of the computing platforms and design methodologies.

Following the aggressive technology scaling trends and the fundamental limits of optical lithography, the gap between the designed layout and what is really fabricated on silicon is increasing. As a consequence, performances predicted during the design implementation may significantly differ from post-silicon measurements. Furthermore, the number of variability sources is also growing as the fabrication processes become more and more complex, and the correlation between different variability sources is also more difficult to predict. Transistor variability of design-related parameters, resulting either from manufacturing fluctuations, or from the device intrinsic atomic nature will increase as technology scales down. However, in spite of all the technology-related effects, the design efforts must be focused at the architectural level to manage the complexity of modern SoC designs. Hence, an alternative design paradigm based on forms of regularity at different levels of abstraction, on structured on-chip communication, and with some application-specific customization, would replace the traditional standard cell-based ASIC design style for a wide range of applications.

II. REGULARITY FOR ACHIEVABLE DESIGNS IN NANOMETER TECHNOLOGIES

The building block and enabler of this architecture-to-silicon design platform will be a reduced library of configurable and regular logic components that are implemented by means of a small number of litho-friendly regular layout shapes. These highly predictable and manufacturable regular fabrics will allow focusing the design efforts at the system level, providing a direct path to physical implementation and silicon fabrication. The regular fabrics will enforce regularity in a bottom-up fashion at the physical design stage (micro regularity), by significantly limiting the total number of layout patterns, and will also impose a top-down regularity by reducing the number of logic components used to implement a given design (macro regularity).

III. VARIATION-TOLERANT AND RELIABLE CIRCUITS

Variability is of great importance, influencing yield and overall chip-level performance, and it can be global (die-to-die, wafer-to-wafer, etc.) or local (intra-die). Advanced process control can effectively address chip-to-chip, wafer-to-wafer, and lot-to-lot variability by minimizing global variations. In contrast, non-systematic within-chip variations cannot be addressed by process control, process design, or process modification; they require far more advanced solutions. There are two approaches to address variability. The first one is an extensive characterization and analysis of both the libraries and design, and is based on Statistical Static Timing Analysis (SSTA), where all variability sources are analyzed statistically to obtain probabilistic results. A complementary approach is to design adaptive circuits capable of tolerating parametric variations, and clockless circuits are ideal candidates. In this talk, we will present a fully-automated design methodology to synthesize desynchronized circuits that exhibit increased variability tolerance and better average-case performance, for a minimal power and area overhead.