TUTORIAL 3
OPTIMIZATION TECHNIQUES FOR
LOW POWER VLSI CIRCUITS

Speakers:

Srinivas Devadas, Massachusetts Institute of Technology, Cambridge, MA, is associate professor of electrical engineering and computer science. His interests span all aspects of the synthesis of VLSI systems, with recent emphasis on computer aids for the synthesis of low-power electronic circuits.

Anantha Chandrakasan, Massachusetts Institute of Technology, Cambridge, MA, is assistant professor of electrical engineering and computer science. He was an architect of the InfoPad low-power wireless terminal, and is a co-author of the book "Low Power CMOS Digital Design".

Sharad Malik, Princeton University, Princeton, NJ, is assistant professor of electrical engineering. His research interests are in the synthesis of VLSI circuits, embedded systems design, CAD techniques for low-power circuits, and software-level power analysis and optimization.

Background: This tutorial is for researchers and practitioners interested in the optimization of VLSI designs for low power. Knowledge of integrated circuit design flow will be helpful.

Description: Power dissipation has become an important parameter in the design of integrated circuits, particularly for portable computers and personal communication systems. This tutorial will describe optimization techniques for low power that can be applied to integrated circuit designs at the circuit, logic, register-transfer, behavioral, system and software levels.

Srinivas Devadas will describe the power dissipation model underlying the optimization methods, and provide background in power estimation. Optimizations to reduce power dissipation at the circuit level will be presented, including transistor reordering and transistor sizing. Transformations to reduce the power dissipation of combinational logic, low-power-driven logic optimization algorithms based on these transformations, and techniques to optimize sequential logic for low power will be described.

Anantha Chandrakasan will present techniques to minimize power consumption at the behavioral and system levels by minimizing power supply voltage and switched capacitance. A key approach combines architecture optimization with voltage scaling; this allows a trade-off between area and power. Algorithmic transformations can be used to significantly reduce power consumption. System-level low-power trade-offs drawn from multimedia portable systems such as the InfoPad will demonstrate that orders of magnitude power reduction are possible.

Since many applications are now implemented as embedded systems (application-specific software running on dedicated processors), power consumption of software also needs to be considered. Sharad Malik will describe techniques for analyzing the power cost of programs and the development of instruction-level power models for some commercial CPUs. Given the ability to evaluate programs in terms of their power/energy costs, it is possible to search the design space in software power optimization. Various techniques for software power optimization will be presented.