On-Die Interconnect and Other Challenges for Chip-Level Multi-Processing

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Abstract

There is increasing interest in chip-level multi-processing, and in this talk I will discuss some the motivations, and some of the challenges in designing such chips. A key component is the on-die interconnect, and we will look at this along with some thoughts on core design, cache architecture, memory bandwidth, power management, error handling, and system scaling.

Bio

Tryggve Fossum is an Intel Fellow, Digital Enterprise Group, and Director of Microarchitecture Development. He is the lead architect for the next generation Xeon server and Intel’s advanced multiprocessing chip architecture. Fossum joined Intel as part of a June 2001 agreement with Compaq Computer Corporation that called for the transfer of microprocessor engineering and design expertise to Intel.

Prior to joining Intel, Fossum held a variety of positions during 28 years of combined service to Compaq and Digital Equipment Corporation. Since 1998, he served as a Compaq Fellow and was lead architect for future versions of the Alpha microprocessor. From 1991 to 1998, Fossum led a team conducting processor and compiler technology research. Prior to this, he was a consulting engineer and helped design several VAX processors for Digital.

Fossum received a Cand Mag degree in Science from the University of Oslo in 1968. He earned his doctorate and master’s degree in mathematics from the University of Illinois in 1972 and 1970, respectively. Fossum completed a post-doctorate program at the University of Illinois in 1973.

Fossum holds 30 patents on various aspects of computer design, including floating point, multithreading and cache organization technologies.