Embedded Tutorial: IC Test Cost Benchmarking

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Abstract:
Driven by the increasing complexity of integrated circuits the pressure on test cost reduction increases exponentially as productivity on chip level progresses according to Moore's Law.
A high-level strategic approach for test cost target setting and planning will be explained. The intention is to keep cost of test constant relative to overall cost of goods sold.
This method has been developed and used at Infineon over the last couple of years to align our location, equipment and productivity target setting.

Key elements of this approach are:
- Consolidation at different levels of analysis is possible.
- Building of peer groups between different product classes for best practice comparison
- Economically relevant benchmark data rather than a pure machine or test time level comparison
- Objective and neutral data base for benchmarking with external partners. Sensitive internal data can not be derived.
- Easy to use tool to judge trade-offs between R&D expenses and production cost.

Description of the approach:
Each product is given a set of basic data which comprises of:
- All steps of the production route.
- Chip size, chips per wafer
- Technology node
- Package type
- Planned yield FE/BE
- Test time
- Index time
- Tester type used

The accounting system reports dedicated cost indications for:
- Wafer level
- Package type
- Test cost per hour by machine

Based on the availability of all relevant information in a manufacturing database it is a very simple task to compute:
- Cost per product
- Cost per product groups, e.g. per product line
- Cost per factory
- Global test cost

It is very helpful to build peer groups of products and compare their relative cost, e.g. all types of GSM transceivers – different product generations or products for different applications. But also peers like DECT to Bluetooth transceivers. The beauty of the concept is in its very concise applicability to an engineer’s individual project as well as for global top down planning.
Once a business plan for a fiscal year is established one can compute global manufacturing expenses bottom up and can compare it to a hypothetical best case if all products in question were at benchmark performance. From there trade-offs between R&D effort and amortization in volume production as well as prioritization can take place and concrete improvement plans can be decided.
For discussions both at a strategic as well as at a concrete product level use of the indicator “Cost of Test / Cost of Goods Sold” (CoT) is recommended. This number is economically very relevant as each percent point improvement directly goes into the bottom of a business unit. Therefore it is also useful in order to assess business cases, i.e. how much R&D investment is justified to gain x percent CoT improvement, or how much volume is needed to ship in order to amortize given R&D efforts?
Trying to keep CoT flat or even lower it over time is a very challenging task to test engineering as it in essence means keeping up with Moore’s Law.
As it is a relative indicator it is perfectly suitable for external, even industry wide benchmarking comparisons. As mentioned above the indicator is economically relevant, but can be shared without disclosing any sensitive information like yield, chip size or margin contribution of your product.

Conclusion:
We would like to demonstrate our approach for target setting and benchmarking with the intention to develop this to a generally accepted industry practice. This shall help all users of this approach to more consistently drive their continuous improvement.