VLSI Design of a High Speed Soft Decision Viterbi Detector

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Abstract

The design of a Viterbi detector for high speed disk drive channels is presented. The detector is a soft decision detector that operates on a time varying trellis based on a matched spectral null code. The design was developed by creating a high level model of the system to resolve high level design issues. Standard design tools were used for logic simulation and layout generation. The design has been fabricated and verified to be fully functional.

1 Introduction

Presently, partial response channels are being used in high end disk drive recording channels due to their increased recording densities. Future channels may employ coding techniques such as a Matched Spectral Null (MSN) codes. However, in practical codes, the predicted coding gain may not be achieved due to the effect of catastrophic sequences. This problem is avoided in this design through the use of a time varying trellis.

1.1 Viterbi Detector

A finite precision model was developed from the high level description of the system. Error rate measurements were performed to verify the specifications. This finite precision model supports the ability to vary the precision of the arithmetic and observe the error rate performance. It was determined that 4 bit quantization is sufficient to achieve the expected 3dB coding gain of the MSN code. A path memory depth of 16 bits is required to achieve the 3dB gain. Two's complement arithmetic was used to avoid normalization requirements.

1.2 VLSI Design

The design was based on a 0.7um standard cell library. Post route simulations indicated that the chip would operate at 75Mhz typical and 50Mhz worst case. The prototype chip has 11k NAND equivalent gates and an area of 3.63mm by 3.27mm including IO pads. Figure 1 shows a block diagram of the implemented prototype.

2 Prototype Measurements

The prototype chips have been fabricated. The designed 3dB gain of the MSN Viterbi decoded data over normal PR4 Viterbi decoded data has been measured and is shown in figure 2. The maximum operating frequency of the IC's was measured and the device was verified to operate at greater than 100Mhz with 4.5V supplies. The performance of the IC with various ADC resolutions was measured and it was confirmed that 4 bit quantization is sufficient to achieve the required coding gain.

Figure 1: Prototype VLSI block diagram

Figure 2: Measured Errorrate of Prototype IC