Message from the Symposium Chairs

Organizing Committee

Program Committee

Keynote Talk

The Evolving Role of Test ... it is now a “Value Add” Operation

Phil Nigh, IBM

Session 1: Defect and Fault Tolerance

Using TMR Architectures for Yield Improvement

J. Vial, A. Bosio, P. Girard, C. Landrault, S. Pravossoudovitch, and A. Virazel

Module Grouping for Defect Tolerance in Nanoscale Memory

Yoonjae Huh and Yoon-Hwa Choi

Coping with Obsolescence of Processor Cores in Critical Applications

Francesco Abate and Massimo Violante

A Low-Power Safety Mode for Variation Tolerant Systems-on-Chip

David Wolpert and Paul Ampadu

Session 2: Dependability Analysis and Evaluation

Built-In Self-Diagnostics for a NoC-Based Reconfigurable IC for Dependable Beamforming Applications

Oscar J. Kuiken, Xiao Zhang, and Hans G. Kerkhoff

Network Fault Model for Dependability Assessment of Networked Embedded Systems

Franco Fummi, Davide Quaglia, and Francesco Stefanni

Obtaining Microprocessor Vulnerability Factor Using Formal Methods

Syed Z. Shazli and Mehdi B. Tahoori

System Reliabilities when Using Triple Modular Redundancy in Quantum-Dot Cellular Automata

Timothy J. Dysart and Peter M. Kogge
### Invited Talk

Error Detection and Tolerance for Scaled Electronic Technologies ................................................................. 83  
*Kartik Mohanram, Rice University*

### Session 3: Hot Topics

Hardware Trojan Detection and Isolation Using Current Integration and Localized Current Analysis .......................................................... 87  
*Xiaoxiao Wang, Hassan Salmani, Mohammad Tehranipoor, and Jim Plusquellec*

Built-In Proactive Tuning System for Circuit Aging Resilience ........................................................................... 96  
*Nimay Shah, Rupak Samanta, Ming Zhang, Jiang Hu, and Duncan Walker*

*Andrey Zykov and Gustavo de Veciana*

Impact of Technology and Voltage Scaling on the Soft Error Susceptibility in Nanoscale CMOS .......................................................... 114  
*Vikas Chandra and Robert Aitken*

### Session 4: Design for Testability

Enhancing Silicon Debug via Periodic Monitoring ......................................................................................... 125  
*Joon-Sung Yang and Nur A. Touba*

A Digital BIST for Phase-Locked Loops ........................................................................................................... 134  
*Kevin Sliech and Martin Margala*

On Optimizing Fault Coverage, Pattern Count, and ATPG Run Time Using a Hybrid Single-Capture Scheme for Testing Scan Designs ......................................................................................... 143  
*Shianling Wu, Laung-Terng Wang, Zhigang Jiang, Jiayong Song, Boryau Sheu, Xiaoqing Wen, Michael S. Hsiao, James C.-M. Li, Jiun-Lang Huang, and Ravi Apte*

Analyzing the Impact of Fault-Tolerant BIST for VLSI Design ........................................................................... 152  
*W. Robert Daasch, Saurabh Jain, and David Armbrust*

### Invited Talk

Targeting “Zero DPPM” – Can We Ever Get There? ......................................................................................... 163  
*Nilanjan Mukherjee, Mentor Graphics*

### Session 5: Posters

A BIST Technique for Crosstalk Noise Detection in FPGAs ........................................................................... 167  
*Waleed K. Al-Assadi and Sindhu Kakarla*

A Fault Tolerance Aware Synthesis Methodology for Threshold Logic Gate Networks .......................................................... 176  
*Manoj Kumar Goparaju, Ashok Kumar Palaniswamy, and Spyros Tragoudas*

A Framework to Evaluate the Trade-Off among AVF, Performance and Area of Soft Error Tolerant Microprocessors ........................................................................................................... 184  
*Rui Gong, Kui Dai, and Zhiying Wang*

A Power Efficient Masking Technique for Design of Robust Embedded Systems against SEUs and SETs ........................................................................................................... 193  
*Mahdi Fazeli and Seyed Ghassem Miremadi*
Can Knowledge Regarding the Presence of Countermeasures Against Fault Attacks
Simplify Power Attacks on Cryptographic Devices? .................................................................202
   Francesco Regazzoni, Thomas Eisenbarth, Luca Breveglieri, Paolo Ienne, and Israel Koren
Modeling and Evaluation of Threshold Defect Tolerance .............................................................211
   Zachary Patitz and Nohpill Park
Defect Tolerance for a Capacitance Based Nanoscale Biosensor ..................................................220
   Glenn H. Chapman and Vijay K. Jain
Fault Detection of Bloom Filters for Defect Maps ........................................................................229
   Jae-Young Choi and Yoon-Hwa Choi
Fault Tolerant Schemes for QCA Systems ......................................................................................236
   Xiaojun Ma and Fabrizio Lombardi
On Reducing Circuit Malfunctions Caused by Soft Errors ..........................................................245
   Ilia Polian, Sudhakar M. Reddy, Irith Pomeranz, Xun Tang, and Bernd Becker
Realization of L2 Cache Defect Tolerance Using Multi-bit ECC ..................................................254
   Hongbin Sun, Nanning Zheng, and Tong Zhang
Selective Hardening of NanoPLA Circuits ...................................................................................263
   Ilia Polian and Wenjing Rao
Soft Error Hardened FF Capable of Detecting Wide Error Pulse ..................................................272
   Shuangyu Ruan, Kazuteru Namba, and Hideo Ito
XOR-Based Low Cost Checkers for Combinational Logic ..........................................................281
   Carlos Arthur Lang Lisboa and Luigi Carro
Minimization of CTS of k-CNOT Circuits for SSF and MSF Model ..............................................290
   Muhammad Ibrahim, Ahsan Raja Chowdhury, and Hafiz Md. Hasan Babu

Keynote Talk

Architectural Vulnerability Factor (or, Does a Soft Error Matter?) ..................................................301
   Shubu Mukherjee, Intel

Session 6: Reliability and Fault Tolerance

Automatic Detection of In-Field Defect Growth in Image Sensors ..............................................305
   Jenny Leung, Glenn H. Chapman, Israel Koren, and Zahava Koren
Material Fatigue and Reliability of MEMS Accelerometers .......................................................314
   Xingguo Xiong, Yu-Liang Wu, and Wen-Ben Jone
Fault-Tolerance with Graceful Degradation in Quality: A Design Methodology and its Application to Digital Signal Processing Systems .........................................................323
   Nilanjan Banerjee, Charles Augustine, and Kaushik Roy
Design Space Exploration for the Design of Reliable SRAM-Based FPGA Systems ..................332
   Cristiana Bolchini and Antonio Miele
Session 7: Error Detection and Correction (1)

A Low Cost Scheme for Reducing Silent Data Corruption in Large Arithmetic Circuits.................343
Abhisek Pan, James W. Tschanz, and Sandip Kundu

Adaptive Error Control for NoC Switch-to-Switch Links in a Variable Noise Environment ...........352
Qiaoyan Yu and Paul Ampadu

Arbitrary Error Detection in Combinational Circuits by Using Partitioning.................................361
Osnat Keren, Ilya Levin, Vladimir Ostrovsky, and Beni Abramov

Error Detect Logic Resulting in Faster Address Generate and Decode for Caches .........................370
Prashant D. Joshi

Invited Talk

A Case Study of ATPG Delay Path Performance Based on Measured Power Rail Integrity.............381
Zahi Abuhamdeh, Transwitch

Session 8: Testing Techniques

ATPG Heuristics Dependant Observation Point Insertion for Enhanced Compaction
and Data Volume Reduction .................................................................385
Santiago Remersaro, Janusz Rajski, Thomas Rinderknecht, Sudhakar M. Reddy,
and Irith Pomeranz

Detection of Transistor Stuck-Open Faults in Asynchronous Inputs of Scan Cells .........................394
Fan Yang, Sreejit Chakravarty, Narendra Devta-Prasanna, Sudhakar M. Reddy,
and Irith Pomeranz

Efficient Determination of Fault Criticality for Manufacturing Test Set Optimization .................403
Yiwen Shi, Kellie DiPalma, and Jennifer Dworak

Core Test Wrapper Design to Reduce Test Application Time for Modular SoC Testing .................412
Hyunbean Yi and Sandip Kundu

Session 9: Panel

Zero Defects: How Can We Get There?
Organizer: M. Tehranipoor, University of Connecticut

Invited Talk

Computing at the Nanoscale .................................................................423
John E. Savage, Brown University
Session 10: Error Detection and Correction (2)

A Generalized Approach for the Use of Convolutional Coding in SEU Mitigation ........................................ 427
Laura Frigerio, Matteo Alan Radaelli, and Fabio Salice

A Novel Error Detection and Correction Technique for RNS Based FIR Filters ........................................ 436
S. Pontarelli, G.C. Cardarilli, M. Re, and A. Salsano

An Asymmetric Checkpointing and Rollback Error Recovery Scheme for Embedded Processors ........................................ 445
Hamed Tabkhi, Seyed Ghassem Miremadi, and Alireza Ejali

Design and Evaluation of a Timestamp-Based Concurrent Error Detection Method (CED) in a Modern Microprocessor Controller ........................................ 454
Michail Maniatakos, Naghmeh Karimi, Yiorgos Makris, Abhijit Jas, and Chandra Tirumurti

Session 11: Testing for Timing and Parametric Failures

Novel On-Chip Clock Jitter Measurement Scheme for High Performance Microprocessors .................. 465
Cecilia Metra, Martin Omaña, TM Mak, Asifur Rahman, and Simon Tam

Prioritization of Paths for Diagnosis ......................................................................................................... 474
Rajsekhar Adapa and Spyros Tragoudas

Delay Fault Testability on Two-Rail Logic Circuits .......................................................................................... 482
Kazuteru Namba and Hideo Ito

Diagnosis of Analog Circuits by Using Multiple Transistors and Data Sampling ............................................. 491
Yukiya Miura and Jiro Kato

Invited Talk

Design for Test Challenges of High Performance/Low Power Microprocessors ............................................. 503
Kamran Zarrineh, AMD

Invited Talk

Defect-Tolerant Hybrid CMOS/Nanoelectronic Circuits .............................................................................. 504
Konstantin K. Likharev, Stony Brook University

Session 12: Emerging Technologies

A Statistical Model for Assessing the Fault Tolerance of Variable Switching Currents for a 1Gb Spin Transfer Torque Magnetoresistive Random Access Memory ........................................ 507
Yoshiaki Asao, Masayoshi Iwayama, Kenji Tsuchida, Akihiro Nitayama, Hiroaki Yoda, Hisanori Aikawa, Sumio Ikegawa, and Tatsuya Kishi

A Tile-Based Error Model for Forward Growth of DNA Self-Assembly ....................................................... 516
Masoud Hashempour, Zahra Mashreghian Arani, and Fabrizio Lombardi

Checkpointing of Rectilinear Growth in DNA Self-Assembly ......................................................................... 525
Stephen Frechette, Yong Bin Kim, and Fabrizio Lombardi

Fabrication Variations and Defect Tolerance for Nanomagnet-Based QCA .................................................... 534
Michael Niemier, Michael Crocker, and X. Sharon Hu

Author Index .................................................................................................................................................... 543