Logic Diagnosis and Yield Learning

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Abstract

In the past, logic diagnosis was primarily used to support failure analysis labs. It was typically done on a small sample of defective chips, therefore long processing times, manual generation of diagnostic patterns, and usage of expensive equipment was acceptable. In addition to failure analysis, yield learning relied on test chips and in-line inspection. Recently, sub-wavelength lithography processes have started introducing new yield loss mechanisms at a rate, magnitude, and complexity large enough to demand major changes in the process. Test chips are no longer able to represent the various failure mechanisms originating from critical features. The number of such features is too large to properly represent it on silicon in a cost-effective manner. For new processes it is also impossible to predict all significant features up front. With the decreasing sizes of defects and increasing percentage of invisible ones, in-line inspection data is not always available.

To compensate for fading effectiveness of classical yield learning methods, new solutions are emerging that use logic diagnosis to turn production material into vehicles for yield learning. High-volume diagnosis is combined with the newly emerging field of design for manufacturing to make the analysis layout aware. This new approach offers a lot of advantages but it also presents many challenges from efficient collection of massive amounts of fail log data in production environment, fast and accurate diagnosis in test compression, links to process and lithography simulation, statistical post-processing of the results, and calculation of feature failure rates. Analysis of test data from manufacturing test is a true goldmine of information to calibrate, today largely qualitative, DFM rules and compute yield sensitivity functions. By closing the loop between DFM techniques and the actual defect behavior there is the potential to not only improve yield but also provide validation and calibration of DFM rules.