A NOVEL RAM ARCHITECTURE FOR BIT-PLANE BASED CODING

Bipul Das
Department of ECE
University of Illinois
Chicago - 60607
USA

Swapna Banerjee*
Department of E & ECE
Indian Institute of Technology
Kharagpur - 721302
India

An optimized memory organization has been designed for the hierarchical coding of wavelet subbands. A better economy in time and resources can be accomplished by changing the RAM access pattern and using multiple location access at each clock instant. The bit-planes are distributed along the z-direction and the x−y plane contains 256×256 number of memory elements. The memory plane selection is done by the plane-decoder.

The select line of the plane decoder is a 3-input line, which determines the memory plane to be selected. Each plane has in turn \( N \times N \) memory units, which are addressed by the row and column decoders, composed of 8 number of \( 8 - to - 256 \) decoders. In the worst situation either of 8 rows or 8 columns can be selected simultaneously. The possible combinations of rows and columns are \((1, 8), (2, 4), (4, 2)\) or \((8, 1)\). Selection of 8 columns, for example, implies that 8 addresses should be selected from the column decoder. To accomplish this situation, 8 different \( 8 - to - 256 \) decoders are used. Each of the decoders take an address \((C0 - C7)\), and the corresponding output of the decoders are high (for active high output device). The individual bit-planes of all the decoder output are \( OR \)-ed, e.g., the LSB of all the eight decoders are \( OR \)-ed to get the signal \( col0 \), the MSB are \( OR \)-ed to get \( col255 \) and similarly for other bit-planes too. Similar strategy has been used for row decoding. However, for row decoding along with the \( OR \)-ed output, all the eight inputs are used for data line selection in the RAM.

The output of the storage elements are multiplexed by eight 256 bit bus. For 256 columns, 8 number of 256-bit buses are used as output. In the proposed organization, a switching structure is used for selection of the data-line. 8 data-lines are placed parallelly along each column. For a bit-line, if 8 word lines are high, the corresponding cells will be activated and the data will be transmitted to the data lines.

In a 256 × 256 image, for EZW or SPIHT coding, the conventional RAM requires 32 × 256 × 256 clocks while the proposed RAM structure requires only 8 × 32 × 256 clocks. Thus, the proposed RAM requires much less clocks to read the data for bit-plane coding.

* Author for correspondence, e-mail: swapna@ece.iitkgp.ernet.in, Ph: +91 3222 283500, Fax: +91 3222 255303