Real-Time VLSI Compression for High-Speed Wireless Local Area Networks

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We present a new compact, power-efficient, and scalable VLSI array for the first Lempel-Ziv algorithm to be used in high-speed wireless data communication systems. This is part of a project at the University of Massachusetts to develop reliable and secure high-speed wireless LANs by exploiting novel VLSI technology, communications algorithms and network protocols. For wireless LANs to be seamlessly and transparently integrated with wired LANs, they must support comparable data rates from 10 Mbps (Ethernet) to 100 Mbps (FDDI). Lossless data compression can be used to inexpensively halve the amount of data to be transmitted, thus improving the effective bandwidth of the communication channel and in turn, the overall network performance. Lossless data compression is too complex to implement at the high data rates required by optical networks (1 Gbps). However for wireless networks, the data rate and latency requirement are appropriate for a dedicated VLSI implementation of LZ compression. The nature of wireless networks requires that any additional VLSI hardware also be small, low-power and inexpensive.

Most previous hardware implementations of lossless data compression algorithms require either too many processors or power-hungry content addressable memories (CAM). Software implementations of LZ on even current high-end microprocessors are limited to about 8-16 Mbps. Our architecture uses a novel custom systolic array and a simple dictionary FIFO which is implemented using conventional SRAM. The architecture consists of \( M \) simple processing elements where \( M \) is the maximum length of the string to be replaced with a codeword, which for practical LAN applications, can range from 16 to 32. The systolic cell has been optimized to remove any superfluous state information or logic, thus making it completely dedicated to the task of LZ compression. A prototype chip has been implemented using 2\( \mu \) CMOS technology. Using \( M=32 \), and assuming a 2:1 compression ratio, the system can process approximately 90 Mbps with a 100 MHz clock rate (simulated) thus achieving sufficient performance for all current and most foreseeable wireless LANs. The LZ module contains only 11,000 transistors and consumes only 62 mW, thus allowing it to be inexpensively added to the digital hardware in a wireless LAN transceiver.