A Multi-Layer Channel Router with New Style of Over-the-Cell Routing

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Abstract

This paper discusses a new style of over-the-cell routing, where a new cell structure is introduced. Terminals are located around the horizontal center line in the cell. We regard the region between the central terminals in the upper cell row and ones in the lower cell row as an expanded channel. A new channel router handles that region in a lump where connections to terminals are perfectly achieved by avoiding obstacles in cells. Furthermore, the router shortens the length of polysilicon wires so as to achieve the high-performance circuits. Experimental results show that the router achieves a goal of the size reduction which is predicted according to the theoretical estimation, and that the length of polysilicon wires is dramatically shortened.

1 Introduction

With recent advances in manufacturing technology, it has been made possible to use three or even four layers for interconnections. In the standard cell approach, it is indispensable to extend channel to handle multi-layered regions. Several multi-layer channel routers [1]-[6] have been developed because of effectiveness and high-speed processing of channel routing. In order to reduce channel height still more, the over-the-cell channel routers have been discussed [7]-[14]. In their routing models (except for [14]), terminals have been limited to being placed on outlines of cells, and hence routing region was divided into two regions: channels and regions over the cells. Since the routers should be applied to each of regions individually, the results deeply depend on the selection of nets to be routed over the cells [12]. This selection is a key problem, however, very difficult.

This paper proposes a new style of over-the-cell routing, where a new cell structure is introduced to make good use of cell regions. Terminals exist not only on the top and bottom edges of cells but also around the horizontal center line. We regard the region between the central terminals of the upper and lower cell rows as an expanded channel. The router handles that region in a lump, where connections to central terminals are perfectly achieved by avoiding obstacles in cells. Since it is not necessary to beforehand select a set of nets which will run over the cells, our router can globally perform the routing with minimal channel height. Moreover, from the industrial point of view, the length of polysilicon wires should be shortened in order to achieve the high-performance circuits. Experimental results show that our router achieves a goal of the size reduction which is predicted according to the theoretical estimation, and that the length of polysilicon wires is dramatically shortened as compared with that without the consideration about polysilicon terminals.

2 New cell model

It is assumed that four layers (polysilicon layer: P and three metal layers: M1, M2 and M3) are available to routing. P and M2 (M1 and M3) are used for vertical (horizontal) wiring. For each layer, there is a grid superimposed over the routing region. Wires will run along grid lines in rectilinear fashion. An electrical connection between two wires on adjacent layers is performed by a via. The vias are placed on the cross points of grid lines for layers to be connected.

We introduce a new cell structure shown in Fig. 1. Obstacles may exist in upper and lower outsides of the cell. Its shape is regarded as a rectilinear polygon. Terminals are located not only on the outline of the cell but also around the horizontal center line. Equi-potential terminals are only allowed to be on the same vertical column. In fact, it is rather easy to modify the existing cells into cells of the new structure.

Terminals around the center line are referred to as the central terminals. The terminal of layer L is denoted by the L-terminal. There exist P-terminals only on the outline of the cell. All of central terminals are of M2. An M3 wire can run along any M3 grid lines, since M3 is not used in the cell layout. On the other hand, it is necessary that an M2 wire is routed with avoiding obstacles of M2.

![Fig. 1 New cell structure.](image)

3 Expanded channel

On the basis of the cell model, we consider a new routing region as shown in Fig. 2. This region is called an expanded channel. It is defined to be the maximal rectilinear polygon surrounded by the central terminals and horizontal center lines in the upper and lower cell rows. The lower (upper) half part of the upper (lower) cell row is referred to as the over-the-cell region.

It is assumed that, in the over-the-cell region, only wires of M2 and M3 can be used. The grid lines of M1 and M3 (P and M2) are referred to as tracks (columns). Especially, the partial grid lines of M3 (M2) included in the cell regions are referred to as the cell columns (tracks).
4 Over-the-cell multi-layer routing

4.1 Routing for the expanded channel

Our router acts on the following 4 steps.

Step 1: Specification of channel
Step 2: Routing from central terminals
Step 3: Changing P-terminals to M2
Step 4: Track assignment

In step 1, the expanded channel is defined based on the cell data. Step 2 performs the connections to central terminals with avoiding obstacles in cells. (We will explain the algorithm of Step 2 in 4.2.) In step 3, the P-wires connecting to P-terminals are routed to M2 wires, for as many P-terminals as possible. This layer changing is achieved by using a pattern which is fittedly chosen out of three patterns shown in Fig. 3. The changing is required to make good use of M3 tracks, since an M2 wire can immediately connect to an M3 wire by setting only one via. Moreover, as a result of the changing, the total length of P wires will be shortened. Finally, according to vertical constraints, horizontal wires of subsets are assigned to tracks of M1 and M3 in step 4. The algorithm for the track assignment based on [15] is modified to take account of 3.5-layer routing.

Fig. 3 Patterns of changing P-terminal to M2.

4.2 Routing from central terminals

In order to completely perform the routing from each central terminal, the following two processes are required. The cell columns on which a central terminal is located is denoted by col(i).

Selection of drawing direction: If \( \text{col}(i) \) intersects an obstacle \( R \) for a central terminal \( i \), then we must determine the direction (left or right) to which the routing from \( i \) detours and avoids the obstacle \( R \).

Selection of cell track: We must determine a cell track on which the detour runs in order to avoid an obstacle with taking account of the shape of the obstacle.

For example, consider central terminals \( a, b \) and \( c \) in Fig. 4. The detours for terminals \( a, b \) and \( c \) will run along cell tracks \( T_a, T_b \) and \( T_c \), respectively. The direction of routing from \( a \) and \( b \) is to be the left. On the other hand, the direction of routing from \( c \) is to be the right.

Fig. 4 An example of routing from central terminals.
Consider the routing from central terminals \( a, b, c \) and \( d \) in Fig. 5(a). In S.1, \( QL=(b, c) \), \( QR=(d) \). It is noted that cell track \( T_1 \) is broken by central terminal \( a \). Thus, the detours from central terminals \( b \) and \( c \) to the left side of \( R \) can not be achieved by using \( T_2 \). In S.2, for \( b \), two cell tracks \( T_3 \) and \( T_4 \) are listed up. Four cell columns \( c \)-intersect \( T_1 \) in the left side of \( R \). Since \( col(a)=c_1 \), three cell columns \( c_1-c_3 \) are considered as candidates for the cell column used to detouring from \( b \). In S.3, for \( b, c_1 \) is chosen, since \( c_1 \) is the nearest to \( R \). In the similar way, for \( c, T_2 \) and \( c_2 \) are chosen. As shown in Fig. 5(b), in S.4, the routing from \( d \) is achieved by using \( T_1 \) and \( c_2 \) in the right side of \( R \).

(B) Processing priority of central terminals: In the process for the routing from central terminals, we introduce a priority. Then, the routing from central terminals will be performed completely.

Consider an example shown in Fig. 6. Let \( F_c=(a, b) \) and \( F_b=(c) \). If the routing from central terminals \( a \) and \( b \) is achieved according to the order in the queue \( QL \), then the detour from \( b \) can not be obtained as shown in Fig. 6.

When central terminals are processed in S.2, it is required to consider not only the distance from the left or right edge of an obstacle region \( R \) to each central terminal but also the number of available cell tracks between each central terminal and \( R \).

Let \( t \) be a central terminal and \( R \) be an obstacle region obstructing \( t \). The estimation function \( P(t) \) for central terminal \( t \) is defined as follows:

\[
P(t) = k_1 \cdot N_t(t) + k_2 \cdot L_x(t),
\]

where \( N_t(t) \) is the number of available cell tracks between central terminal \( t \) and the minimum convex rectilinear polygon surrounding obstacle region \( R \), \( L_x(t) \) is the horizontal distance from the left (or right) edge of obstacle region \( R \) to central terminal \( t \), and \( k_1 \) and \( k_2 \) are coefficients \((k_1, k_2 > 0)\). (We say a rectilinear polygon \( D \) is convex if any two points in \( D \) are joined by a rectilinear path in \( D \) with at most one bend.) The central terminals are processed according to the increasing order of values of \( P(t) \).

Let's consider the example in Fig. 6 described before, and assume that \( N_t(a)=2, N_t(b)=1, L_x(a)=1, L_x(b)=3, k_1=10 \) and \( k_2=1 \). Then, \( P(a)=21 \) and \( P(b)=13 \). Thus, central terminal \( b \) is prior to \( a \). As a result, we completely accomplish the routing from both \( a \) and \( b \) with avoiding \( R \) as shown in Fig. 4.

5 Experimental results

The proposed channel router runs on NEC EWS4800/220 workstation (30MIPS). The router has been applied to Deutsch's difficult example (DIFF). Positions of terminals are vertically moved to the inside of cells. The grid intervals of M1, M3 in the conventional channel and M3 in the over-the-cell region are 30, 90 and 120 [unit], respectively. The numbers of the upper and lower cell tracks are 5 and 6, respectively. We generate four patterns (P1-P4), Experimental results are summarized in Table 1. In this table, "no change" represents no "changing P-terminals to M2" process. The router reduces the channel height by 18.8% - 50.0% as compared with no-over-the-cell routing. Furthermore, by changing P-terminals to M2, the channel height is reduced by 7.1% - 15.4% and the total length of wires is dramatically shortened by 86.8% - 88.3% compared with "no change" routing. The result for pattern P2 is shown in Fig. 7, where obstacles are denoted by shaded rectilinear polygons.

The channel router has also been applied to several practical circuits. The grid interval of M3 in the conventional channel (the over-the-cell region) is 1.5 times (2 times) wide as one of M1. Table 2 summarizes the experimental results. Note that, for each circuit, the results of the placement and global routing [16] are common to every routing mode. The over-the-cell routing reduces the die size by 22.6% - 33.3% and 11.2% - 12.9% compared with 2.5-layer routing and 3.5-layer routing without over-the-cell routing, respectively. This reduction is approximately equal to the predicted value. The prediction is made according to the estimation based on the number of necessary tracks in 2.5- and 3.5-layer routing, the number of cell tracks, the rate of obstructed cell columns and the rate of P-terminals. The comparison of the routing modes for DATA3 is shown in Fig. 8.
6 Conclusion

In order to make good use of the over-the-cell regions, we introduced the new cell structure in which terminals are located around the horizontal center line. The proposed router processes the expanded channel between the central terminals in the upper cell row and ones in the lower cell row. The experimental results have proven that the proposed router is sufficiently effective and useful to reduce the die size and to shorten the length of polysilicon wires in a practical point of view.

References


Table 1 Experimental results for DIFF

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<th>Observed cell columns</th>
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Table 2 Experimental results for practical circuits

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Fig. 8 Comparison of routing modes for DATA3.

Table 3 Experimental results for practical circuits

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