Guest Editorial: IEEE Transactions on Computers and IEEE Transactions on Nanotechnology Joint Special Section on Defect and Fault Tolerance in VLSI and Nanotechnology Systems

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With increasing demand for ever smaller, portable, energy-efficient and high-performance electronic systems, scaling of CMOS technology continues. As CMOS scaling approaches physical limits, continued innovation in materials, manufacturing processes, device structures and design paradigms have been necessary. High-κ oxide and metal-gate stack were introduced to address oxide leakage; thin body undoped channels, and multiple-gate structures were introduced to mitigate subthreshold leakage; restricted design rules were introduced to improve layout efficiency; yet CMOS technology continues to be challenged in the areas of device aging and reliability. While CMOS is expected to be the dominant semiconductor technology for the foreseeable future, for reasons that are both technological and financial, alternatives to CMOS technology are attracting attention from the researchers.

A large variety of post-CMOS devices have been proposed, including carbon nanotube (CNT) field-effect transistors (CNT-FETs), graphene field-effect transistors (GFETs), tunnel transistors, graphene nanoribbon tunnel field-effect transistors (GNR-TFET), quantum-dots, and single-electron devices (SET). Newer memory technologies such as resistive random-access memory (Re-RAM) have already become commercial, while memristors, Spin Transfer Torque Random Access Memory (STT-RAM) technologies are progressing at a rapid pace.

In parallel with this evolution of the device landscape, computing architectures as well have seen a relevant evolution, pushed by the rise of multi/many-core processors and the stringent request for energy efficiency. Multi-core processors are now widely used across many application domains spanning from embedded to high performance computing (HPC) and specific multicore architectures like GPGPU and computing architectures as well have seen a relevant evolution. High-performance electronic systems and design paradigms have been necessary. High-κ oxide and metal-gate stack were introduced to address oxide leakage; thin body undoped channels, and multiple-gate structures were introduced to mitigate subthreshold leakage; restricted design rules were introduced to improve layout efficiency; yet CMOS technology continues to be challenged in the areas of device aging and reliability. While CMOS is expected to be the dominant semiconductor technology for the foreseeable future, for reasons that are both technological and financial, alternatives to CMOS technology are attracting attention from the researchers.

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In parallel with this evolution of the device landscape, computing architectures as well have seen a relevant evolution, pushed by the rise of multi/many-core processors and the stringent request for energy efficiency. Multi-core processors are now widely used across many application domains spanning from embedded to high performance computing (HPC) and specific multicore architectures like GPGPU and network processors became dominant in their market segment. The complexity of the memory hierarchy is increased, requiring novel designs such as Non-Uniform Memory Access (NUMA). Communication among the different (heterogeneous) cores of the processor and fostered the evolution of several Network on Chip (NoC) architectures. Indeed, to be able to exploit the benefits of these powerful architectures innovative resource management policies are necessary, solutions able to take into account not only the classical aspects of power and performance, but also reliability, which—for the above-mentioned reasons, has become a key issue not only in critical application environments. More precisely, testing and managing reliability, availability and serviceability (RAS) are the challenges that have become crucial for the success of nanoelectronic circuits and systems. This is the driving motivation for this special section of the IEEE Transactions on Computers and IEEE Transactions on Nanotechnology.

The relevance of this topic and the timeliness of this joint Special Section have elicited great response from the research community. This special section attracted 60 papers, involving 300 reviews by more than 150 expert reviewers with careful attention to avoid any conflict of interest. Consequently, this special section, the result of a large collective effort, is one that we are happy to introduce.

The review process resulted in selection of three papers focused on the nanotechnology that are being published in the Transactions on Nanotechnology. The joint special section of the Transactions on Computers includes 10 additional papers, focused on architectural and system-level aspects of the design of reliable systems, working at different levels of abstraction. Some of the papers in this special section also have companion abstract videos prepared by the authors of the papers. Interested readers can link to the videos through the TC portal page at http://www.computer.org/web/tc

The paper “Non-Blocking Testing for Network-on-Chip” by Letian Huang, Junshi Wang, Masoumeh Ebrahimi, Masoud Daneshtalab, Xiaofan Zhang, Guangjun Li, and Axel Jantsch presents a method for the concurrent testing of multiple routers of a network-on-chip architecture in order to assess their status, that can be executed without blocking or dropping packets, thus not introducing performance penalties in the communications.

The article “Capacitive and Inductive TSV-to-TSV Resilient Approaches for 3D ICs” by Ashkan Eghbal, Pooria M. Yaghini, Siavash Yazdi, Nader Bagherzadeh, and Michael Green discusses capacitive and inductive interaction among Through-Silicon Via wires of 3D integrated circuits. Two
approaches to mitigate these effects are presented, the former to mitigate the capacitive effect, the latter for the inductive one. Michele Favalli and Marcello Dalpasso in the paper “Boolean and Pseudo-Boolean Test Generation for Feedback Bridging Fault” investigate the propagation of oscillations due to feedback bridging faults, and propose a logic-level model of the faulty circuit and two techniques aiming to the generation of high-quality test sequences.

“CoreRank: Redeeming Imperfect Silicon by Dynamically Quantifying Core-Level Healthy Condition of Manycore Processors” by Guihai Yan, Faqiang Sun, Huawei Li, and Xiaowei Li introduces a method for evaluating the degradation of a core in a manycore processor with the aim of allowing a graceful degradation of the system, enabling the exploitation of imperfect cores rather than disabling them. Manycore architectures are also investigated in the article “A Power-Aware Approach for Online Test Scheduling in Many-Core Architectures” by Amir-Mohamad Rahmani, Mohammad-Hashem Haghiyavan, Antonio Miele, Mohammad Fattah, Juha Plosila, Pasi Liljeberg, and Hannu Tenhunen, that presents a power-aware non-intrusive online testing approach for manycore systems. The authors propose an approach to testing that takes into account the power budget, minimizing the delays in the workload execution to schedule software based self-test routines.

Testing is central to another paper of the special section: The paper “Development Flow for On-Line Core Self-Test of Automotive Microcontrollers” by Riccardo Cantoro, Paolo Bernardi, Sergio De Luca, Ernesto Sanchez, and Alessandro Sansonetti discusses the issues related to the development of a Software-Based Self-Test library for the automotive field and proposes a development flow for the generation of a test library in order to ease the task.

The paper “Concertina: Squeezing in Cache Content to Operate at Near-Threshold Voltage” by Alexandra Ferreir, Dario Suarez-Gracia, Jesus Alastraub-Re bene, Teresa Monreal Arnal, and Pablo Ibanez presents a last-level cache (LLC) designed to enable reliable operations at low voltages with conventional SRAM cells, mitigating process variation effects at the cost of a modest storage overhead.

Memory is also the focus of the work presented in the next two papers. Bing-Yang Lin, Cheng-Wen Wu, Mincent Lee, Hung-Chih Lin, Ching-Nen Peng, and Min-Jer Wang in their paper titled “A Local Parallel Search Approach for Memory Failure Pattern Identification” focus on the problem of yield loss caused by critical failure patterns and propose a local parallel search algorithm for efficient memory diagnosis and failure pattern identification. The paper “A Novel Scheme for Tolerating Single Event/Multiple Bit Upsets (SEU/MBU) in Non-Volatile Memories” by Fabrizio Lombardi, Kazutero Namba, Yong-Bin Kim, and Wei Wei proposes a novel scheme for a low-power non-volatile memory to withstand Single Event/Multiple Bit upsets.

The special section is closed by a work that takes into account the specific architecture of Graphics Processing Units (GPUs): The paper titled “Evaluation and Mitigation of Radiation-Induced Soft Errors in Graphics Processing Units” by Paolo Rech, Daniel Oliveira, Laercio Pilla, and Thiago Santini evaluates the neuron sensitivity of memory structures in modern GPUs and discusses the behavior of several fault tolerance techniques (e.g., the adoption of Error-Correcting Codes, Algorithm-Based Fault Tolerance) when applied to GPUs programming.

The guest editors would like to thank the reviewers for the quality and timeliness of their reviews. The reviewers have helped to raise the quality of the final submissions of this issue through their quality feedback. They thank the authors for their patience, diligence and dedication at all stages of the review process. Finally, they are grateful to the Editor-in-Chief of the IEEE Transactions on Computers, Dr. Paolo Montuschi, and the Editor-in-Chief of the IEEE Transactions on Nanotechnology, Dr. Fabrizio Lombardi, for making this joint Special Section possible.

Sincerely,

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GuestEditors

Cristiana Bolchini received the degree in Electronic Engineering and the PhD in Automation and Computing Engineering from Politecnico di Milano, where she is now a Professor. Her research interests cover the areas of design and analysis of digital system with a specific focus on dependability, reconfigurable systems and context-aware data design and management. She has authored more than 100 papers in these areas and serves on the Technical Program committees of several conferences focused on reliable systems. She has served as an Associate Editor of the IEEE Transactions on Computers and as an Associate Editor-in-Chief of the IEEE Transactions on Emerging Topics in Computing.

Sandip Kundu is a professor in the Department of Electrical and Computer Engineering at the University of Massachusetts, Amherst. Previously, he was a principal engineer at Intel Corporation and a research staff member at IBM Corporation. He has published more than 200 papers and holds 12 patents and has given more than a dozen tutorials at conferences. He was the technical program chair of ICCD in 2000, program co-chair of ATS in 2011, ISVLSI in 2012 and 2014, DFTS in 2014, and general chair of ICCD in 2001 and co-general chair of VLSI in 2005 and DFTS in 2015. He has also been a distinguished visitor of the IEEE Computer Society. He has served as an associate editor of the IEEE Transactions on Computers, IEEE Transactions on VLSI, and ACM Transactions on Design Automation. Currently, he serves as an associate editor of the IEEE Transactions on Dependable and Secure Computing. He is a fellow of the IEEE and JSPS.

Salvatore Pontarelli received the master’s degree from the University of Bologna in 2000 and the PhD degree in microelectronics and telecommunications from the University of Rome Tor Vergata in 2003. Currently, he works as a senior hardware design engineer at CNIT (Italian Consortium of Telecommunication), in the research unit of the University of Rome Tor Vergata. In the past, he has worked with the National Research Council (CNR), the Department of Electronic Engineering of University of Rome Tor Vergata, the Italian Space Agency (ASI), the University of Bristol, and has been a consultant for various Italian and European companies for projects related to digital design and to fault tolerance in digital systems. He has published more than 100 papers in archival journals (mostly IEEE) and peer-reviewed conferences, and has served as a reviewer for many IEEE sponsored journals and conferences. He has been general chair of the second MEDIAN Workshop, a program chair of the IEEE Symposium on Defect and Fault Tolerance in VLSI systems, in 2014 and a general chair of the IEEE Symposium on Defect and Fault Tolerance in VLSI systems in 2015. He has been a guest editor for Embedded Hardware Design Journal—Microprocessors and Microsystems, and he is an associate editor for the IEEE Transactions on Nanotechnology.