Errata to “Process Variation-Aware Nonuniform Cache Management in a 3D Die-Stacked Multicore Processor”

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Index Terms—Process variation, 3D die stacking, DRAM, NUCA

In our article that appeared in November, 2013 [1], a production error occurred which resulted in the misalignment of Fig. 13, Fig. 14, Fig. 15, Fig. 16, Fig. 17, and Fig. 18 with their captions, starting from Fig. 13 to Fig. 18. As a result, a correct Fig. 13 is missing, and Fig. 18 repeats Fig. 19. We regret that this has happened. The correct figures with their corresponding captions are shown as follows.

REFERENCES


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Fig. 16. Performance of the improved intracolumn two-tier migration technique, normalized to the ideal baseline.

Fig. 17. Energy-delay product results.

Fig. 18. DRAM subbank latency distribution under three PV configurations.