State of the Journal

Albert Y. Zomaya

Welcome to the January issue of TC. This is going to be another exciting year for us. In this issue I will share with you some of the developments that TC is undertaking.

During 2011, TC has maintained its position as a leading and prestigious publication in the field of computing. The number of manuscript submissions (inclusive of Special Sections) was 872 papers (at the time of writing this editorial in November 2011). The number of papers published was 139 papers plus approximately 140 additional papers were posted online as preprints (with an acceptance rate around 23.6 percent). Going by the number of papers received to date, I can guarantee you that 2012 will be another successful year for TC.

The page budget stood at 1872 pages during 2011, which will maintained at the same level in 2012. As a measure of overall timely review, over the last 12 months the delay encountered from submission to first notification has been under three months. We are striving to improve this turnaround period and I am positive that this will be achieved due to the effort of the great team that we have. I would like to extend my gratitude to the wonderful team of Associate Editors, Guest Editors, reviewers, and IEEE Computer Society staff. Of course, we cannot forget our loyal authors and readers. I thank you all for such a job well done!

A number of special sections have been published in 2011. TC does not publish special issues and the special sections are the mechanism used to enable the organization of mini special issues to publish on topical themes that are of importance to our readership. The themes covered in 2011 were Dependable Computer Architecture, Computer Arithmetic, Chips and Architectures for Emerging Technologies and Applications, Science of Design for Safety Critical Systems, and Concurrent Online Testing and Error/Fault Resilience of Digital Systems.

The organization of such special sections will continue in 2012. Information on the scheduled special sections appears on the journal’s homepage (please see http://www.computer.org/portal/web/tc). I look forward to the participation of our community in these special sections.

In 2011, TC celebrated its 60th anniversary. Many of our past and current volunteers joined in these celebrations. One of these activities was to publish quotes in the journal web page from researchers reminiscing about their involvement with TC (see http://www.computer.org/portal/web/tc/60th). This page will remain active throughout 2012. So, please feel free to keep on sending me your congratulatory quotes and I will endeavor to have them published.

In late 2011, a few of our Associate Editors concluded their tenure: Sonia Fahmy, Tarek El-Ghazawi, Sunil Khatri, Anna Lysyanskaya, and Igor Markov. I would like to express our thanks to these colleagues for all their professionalism and hard work and wish them well with their future endeavors.

Also, in 2012 several new Associate Editors have joined our team: Eui-Young Chung, Petru Eles, Vincenzo Eramo, Masahiro Fujita, Teofiló F. González, Michael Hsiao, Niraj K. Jha, Cristina Nita-Rotaru, Manish Parashar, Gang Qu, Sanjay Ranka, Francisco Rodríguez-Henríquez, Eric Rotenberg, Berk Sunar, Zahir Tari, Mateo Valero, and Julio Villalba-Moreno.

These colleagues were chosen through an extensive selection process which was approved by the IEEE Computer Society. I would like to welcome them to the board and I am sure their presence will contribute to the continued success of TC.

Please feel free to send me your suggestions and recommendations. I welcome your ideas and suggestions on ways in which we can improve TC. I also look forward to receiving your technical submissions.

One last development that I would like share with you is our multimedia center (see http://www.computer.org/portal/web/tc/multimedia) that is an exciting new development that I would like to encourage you all to contribute it. We are hoping to grow our multimedia center in 2012 with the help our community.

Albert Y. Zomaya
Editor-in-Chief
Eui-Young Chung received the BS and MS degrees in electronics and computer engineering from Korea University, Seoul, in 1988 and 1990, respectively, and the PhD degree in electrical engineering from Stanford University, California, in 2002. From 1990 to 2005, he was a principal engineer with the SoC R&D Center, Samsung Electronics, Yongin, Korea. He is currently a professor with the School of Electrical and Electronic Engineering, Yonsei University, Seoul, Korea. His research interests include system architecture, biocomputing, and VLSI design, including all aspects of computer-aided design with the special emphasis on low-power applications and storage systems, including Solid-State Disks (SSDs). He is a member of the IEEE and the IEEE Computer Society.

Petru Eles is a professor of embedded computer systems with the Department of Computer and Information Science (IDA), Linköping University. His current research interests include embedded systems, real-time systems, electronic design automation, cyber-physical systems, hardware/software codesign, low power system design, fault-tolerant systems, and design for test. He has published a large number of technical papers in these areas and coauthored several books. He received two best paper awards from the European Design Automation Conferences (EURO-DAC) in 1992 and 1994, a best paper award atom the Design Automation and Test in Europe Conference (DATE) in 2005, a best paper award from the International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS) in 2009, and a best presentation award from the 2003 International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS). He has been nominated for best paper awards at the EURO-DAC'95, he Design Automation Conference (DAC) 2001, and the 2003 International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS). He has served as a program committee member for numerous international conferences, such as Design and Test in Europe (DATE, as topic chair), the International Conference on Computer Aided Design (ICCAD, as topic chair), the International Conference on Hardware/Software Codesign and System Synthesis (CODES/ISSS, as TPC chair, general chair, and Steering Committee chair), the Design Automation Conference (DAC), the International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES), the IEEE Real-Time Systems Symposium (RTSS, as special track chair), the Euromicro Conference on Real-Time Systems (ECRTS), the IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), the Euromicro Symposium on Digital Systems Design (DSD), the ACM Conference on Embedded Software (EMSOFT), and the Symposium on Embedded Systems for Real-Time Multimedia (ESTIMedia, as TPC chair). He is an associate editor of the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems and of the IET Proceedings—Computers and Digital Techniques. He was an IEEE CAS Distinguished Lecturer from 2004-2005.

Vincenzo Eramo received the "Laurea" degree in electronics engineering in 1995 and the "Dottorato di Ricerca" (PhD) in information and communications engineering in 2001, both from the University of Roma "La Sapienza." From June 1996 to December 1996 he was a researcher at the Scuola Superiore Reiss Romoli. In 1997, he joined the Fondazione Ugo Bordoni as a researcher in the Telecommunication Network Planning group. From November 2002 to July 2005 he was an assistant professor in the INFOCOM Department of the University of Rome "La Sapienza," where he was an aggregate professor from 2005 to 2010. Since July 2010 he has been an aggregate professor in the Department of Information Engineering, Electronics and Telecommunications (DIET). His research activities have been carried out as a local coordinator in the framework of MIUR national projects (EURO, BORA-BORA, SFINGI) and European Union international projects (e-PhotonONe+, BONE, TREND). He was chairman of the IEEE ICC 2003 and IEEE ICC 2011. His research areas are on queuing theory, resource dimensioning techniques in telecommunication networks, all-optical networks, and Internet switching architectures. His current research interests are focused on the definition and performance evaluation of routing techniques and technologies to reduce the power consumption in telecommunication networks. His homepage is available at http://net.infocom.uniroma1.it/homepages/eramov.htm

Masahiro Fujita received the PhD degree from the University of Tokyo in 1985. He is a professor in the VLSI Design and Education Center (VDEC) at the University of Tokyo. Prior to joining the University of Tokyo in 2000, he was director of CAD at Fujitsu Laboratories of America for six years. He has done innovative work in the areas of digital design verification, synthesis, and testing. He has coauthored 10 books, and has more than 250 publications. He has participated in and chaired many prestigious conferences in CAD and VLSI design. He was and has been an associate editor for the IEEE Transactions on CAD, ACM Transactions on Embedded Computing Systems (TECS), ACM Transactions on Storage (TOS), and Formal Methods in System Design: An International Journal (Springer).
Teofilo Gonzalez received the BSc degree in computer science from the ITESM Mexico in 1972 and PhD degree from the University of Minnesota in 1975. He has been a member of the faculty at OU, Penn State, and UT Dallas, and has spent sabbatical leaves in Mexico (ITESM) and The Netherlands (Utrecht). Since 1984 he has been a professor of computer science at the University of California Santa Barbara (UCSB). His research contributions include algorithms for message dissemination problems, scheduling, computer-aided design, computational geometry, and other problems. His most cited contributions include the first nonapproximability results, open shop scheduling algorithms, preemtive scheduling, (best possible) clustering algorithms, etc. He has served as program committee chair for several conferences, and editor (and guest editor) of several publications. He edited the Handbook on Approximation Algorithms and Metaheuristics. This handbook is the only one in the area, and includes contributions from top researchers from all over the world. He is a fellow of IASTED, has received three teaching awards at UCSB, and serves as a commissioner (CAC) for ABET Inc. His research interests include sequential and parallel algorithms, approximation algorithms, message dissemination, multicasting, graph algorithms, job scheduling, computational geometry, VLSI routing, and placement.

Michael S. Hsiao received the BS degree in computer engineering (highest honors) and the MS and PhD degrees in electrical engineering from the University of Illinois at Urbana-Champaign in 1992, 1993, and 1997, respectively. He was a visiting scientist at NEC USA in Princeton, New Jersey, during the summer of 1997, and during the summer of 2002, he was a visiting professor at Intel, Santa Clara, California. Between 1997 and 2001, he was an assistant professor in the Department of Electrical and Computer Engineering, Rutgers, the State University of New Jersey, Piscataway. Between 2001 and 2006, he was an associate professor in the Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg. Since 2006, he has been a professor in the same department. He and his research group have published more than 200 refereed journal and conference papers. He has served on the program committee for more than 60 IEEE International Conferences and Workshops, in addition to serving as an associate editor on the ACM Transactions on Design Automation of Electronic Systems, as well as on the editorial boards of several journals. He was a recipient of the Digital Equipment Corporation Fellowship, the McDonnell Douglas Scholarship, the National Science Foundation CAREER Award, and is recognized for the most influential papers in the first 10 years (1998-2007) of the Design Automation and Test Conference in Europe (DATE). His research interests include test generation, design for test, diagnosis, hardware security, design verification, design validation, formal verification, formal methods, equivalence checking, and model checking. He is a senior member of the IEEE.

Niraj K. Jha received the BTech degree in electronics and electrical communication engineering from the Indian Institute of Technology, Kharagpur, India in 1981, the MS degree in electrical engineering from the State University of New York at Stony Brook in 1982, and the PhD degree in electrical engineering from University of Illinois at Urbana-Champaign in 1985. He is a professor of electrical engineering at Princeton University. He has served as the Editor-in-Chief of the IEEE Transactions on VLSI Systems and an associate editor of the IEEE Transactions on Circuits and Systems I and II, IEEE Transactions on Computer-Aided Design, IEEE Transactions on VLSI Systems, and Journal of Electronic Testing: Theory and Applications. He is currently serving as an associate editor of the Journal of Low Power Electronics and journal of Nanotechnology. He has also served as the program chairman of the 1992 Workshop on Fault-Tolerant Parallel and Distributed Systems, the 2004 International Conference on Embedded and Ubiquitous Computing, and the 2010 International Conference on VLSI Design. He has served as the director of the Center for Embedded System-on-a-Chip Design funded by the New Jersey Commission on Science and Technology. He is the recipient of the AT&T Foundation Award and NEC Preceptorship Award for research excellence, NCR Award for teaching excellence, and Princeton University Graduate Mentoring Award. He has coauthored or coedited five books, Testing and Reliable Design of CMOS Circuits (Kluwer, 1990), High-Level Power Analysis and Optimization (Kluwer, 1998), Testing of Digital Systems (Cambridge University Press, 2003), Switching and Finite Automata Theory, third edition (Cambridge University Press, 2009), and Nanoelectronic Circuit Design (Springer, 2010). He has also authored 12 book chapters. He has authored or coauthored more than 350 technical papers. He has coauthored 14 papers, which have won various awards. These include the Best Paper Award at ICCD ’93, FTCS ’97, ICVLSID ’98, DAC ’99, PDCS ’02, ICVLSID ’03, CODES ’06, ICCD ’09, and CLOUD ’10. A paper of his was selected for “The Best of ICCAD: A collection of the best IEEE International Conference on Computer-Aided Design papers of the past 20 years,” two papers by IEEE Micro as one of the top picks from the 2005 and 2007 Computer Architecture conferences, and two others as being among the most influential papers of the last 10 years at the IEEE Design Automation and Test in Europe Conference. He has coauthored another five papers that have been nominated for best paper awards. He has received 13 US patents. His research interests include FinFETs, low power hardware/software design, computer-aided design of integrated circuits and systems, digital system testing, and secure computing. He has given several keynote speeches in the area of nanoelectronic design and test. He is a fellow of the IEEE and the ACM.
Cristina Nita-Rotaru is an associate professor in the Department of Computer Science at Purdue University, where she established the Dependable and Secure Distributed Systems Laboratory (DS^2) and is a member of the Center for Education and Research in Information Assurance and Security (CERIAS). Her research lies at the intersection of information security, distributed systems, and computer networks. The overarching goal of her work is designing and building practical distributed systems and network protocols that are robust to failures and attacks while coping with the resource constraints existing in computing systems and networks. She was a recipient of the National Science Foundation Career Award in 2006 and a recipient of the Purdue Teaching for Tomorrow Award in 2007. She has served on the technical program committee of numerous conferences in security, networking, and distributed systems. She is currently an associate editor for the *ACM Transactions on Information and System Security*. She is currently serving as an assistant director for CERIAS. Her research interests include security in computer networks and distributed systems. She is a senior member of the IEEE and a member of the IEEE Computer Society and the ACM.

Manish Parashar received the BE degree from Bombay University, India, and the MS and PhD degrees from Syracuse University. He is a professor of electrical and computer engineering at Rutgers University. He is also a founding director of the Center for Autonomic Computing and The Applied Software Systems Laboratory (TASSL), and associate director of the Rutgers Center for Information Assurance (RUCIA). His research interests are in the broad area of parallel and distributed computing and include computational and data-enabled science and engineering, autonomic computing, and power/energy management. A key focus of his research is on addressing the complexity of large-scale systems and applications through programming abstractions and systems. He has published more than 350 technical papers, serves on the editorial boards and organizing committees of a large number of journals and international conferences and workshops, and has deployed several software systems that are widely used. He has also received numerous awards and is a fellow of the IEEE, a member of the IEEE Computer Society, and a senior member of ACM. For more information please visit http://nsfcc.ac.rutgers.edu/people/parashar/.

Gang Qu received the PhD degree in computer science from the University of California Los Angeles in 2000. He is currently an associate professor in the Electrical and Computer Engineering Department and the Institute for Systems Research at the University of Maryland. He works on energy efficient design of computing devices and hardware-related security and trust problems. He has published more than 100 journal articles and conference papers in these areas and won two best paper awards from MobiCom ’01 and ASAP ’06. He is the cofounder of the Maryland Embedded System Research Lab and a member of the Maryland Cybersecurity Center and wireless sensor lab. He has been involved in organizing many international symposiums, conferences, and workshops sponsored by professional organizations (most IEEE and/or ACM sponsored or cosponsored). He served as the technical program committee cochair of the ACM/IEEE Great Lakes Symposium on VLSI in 2005, the general cochair in 2006, and has been on the steering committee since then. Since 1999, he has been an active reviewer for more than a dozen scientific journals and magazines, including *IEEE Embedded System Letters*, *IEEE Transactions on CAD of Integrated Circuits and Systems*, *IEEE Transactions on Circuits and Systems*, *IEEE Transactions on Information Forensics & Security*, *IEEE Transactions on Mobile Computing*, *IEEE Transactions on Multimedia*, *IEEE Transactions on Networking*, *IEEE Transactions on Signal Processing*, *IEEE Transactions on VLSI Systems*, *Computer magazine*, and *IEEE Design and Test* magazine. He served as the guest editor for a special issue of the *EURASIP Journal on Embedded Systems* in 2005. He is currently an associate editor for *IEEE Embedded Systems Letters and Integration, the VLSI Journal*. He is a senior member of the IEEE.

Sanjay Ranka received the PhD degree in computer science from the University of Minnesota in 1988 and the B.Tech degree in computer science from IIT, Kanpur, India in 1985. He is a professor in the Department of Computer Science at the University of Florida. Most recently, he was the chief technology officer at Paramark, where he developed real-time optimization software for optimizing marketing campaigns. He has also held tenured faculty positions at Syracuse University and as a researcher/visitor at the IBM T.J. Watson Research Labs and Hitachi America Limited. He has coauthored two books: *Elements of Neural Networks* (MIT Press) and *Hypercube Algorithms* (Springer Verlag), 75+ journal articles, and 125+ refereed conference articles. He serves on the editorial board of the *Journal of Parallel and Distributed Computing* and is a past member of the Parallel Compiler Runtime Consortium and the Message Passing Initiative Standards Committee. He was one of the main architects of the Syracuse Fortran 90D/HPF compiler. He is a fellow of the IEEE and AAAS, and a member of the IFIP Committee on System Modeling and Optimization. He serves as a member of the CTSA Biomedical Informatics Committee and member of High Performance Computing at the University of Florida. His research interests include data mining, informatics, energy efficient computing, high performance computing, parallel computing, multicore computing, and GPU computing.
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Eric Rotenberg received the BS degree in electrical engineering in 1991 and the MS and PhD degrees in computer sciences 1996 and 1999 respectively from the University of Wisconsin–Madison. He is a professor of electrical and computer engineering at North Carolina State University. From 1992 to 1994, he participated in the design of IBM’s AS/400 computer in Rochester, Minnesota. His research is in the area of computer architecture with an emphasis on processor architecture. His group is currently promoting the widespread proliferation of microarchitecturally diverse cores for exploiting diverse instruction level behavior within and across programs. To this end, his group is developing open-source tools for automatically generating RTL designs of whole superscalar processors.

Berk Sunar received the BSc degree in electrical and electronics engineering from Middle East Technical University in 1995 and his PhD degree in electrical and computer engineering from Oregon State University in December 1998. In Fall 2000 he joined Worcester Polytechnic Institute (WPI), where he currently serves as an associate professor. He heads the Cryptography and Information Security Laboratory (CRIS Lab) at WPI. He received the National Science Foundation CAREER award in 2002. He organized the Cryptographic Hardware and Embedded Systems Conference (CHES) in 2004 in Cambridge, Massachusetts, and served as a CHES steering committee member for a number of years. He was the coeditor of the CHES ‘05 and WAIFI ’07 Workshops. He is also a founding steering committee member of the International Workshop of Applications of Finite Fields (WAIFI). In 2010 he served as a coeditor on the IACR special issue of the Journal of Cryptology on Hardware Security. Currently, he is serving as an associate editor for the Springer Journal of Cryptographic Engineering. He is a member of the IEEE Computer Society and the International Association of Cryptologic Research professional societies. His research interests include applied cryptography, physical security, computer arithmetic, and architecture. He has published more than 50 papers in select peer-reviewed journals and conference proceedings. He was coeditor of two books published in the Lecture Notes in Computer Science series of Springer Verlag Publishers.

Zahir Tari graduated with an undergraduate degree in mathematics from USTHB, Algeria, in June, 1984, the master’s degree in operational research from the University of Grenoble, France, June, 1985, and the PhD degree in computer science from the University of Grenoble, France, December, 1989. He is a professor of distributed systems at RMIT University. Later he joined the Database Laboratory at EPFL, Swiss Federal Institute of Technology, 1990-1992, moved to QUT (Queensland University of Technology), 1993-1995, and has been RMIT (Royal Melbourne Institute of Technology) since 1996. He is the head of the DSN (Distributed Systems and Networking) at the School of Computer Science and IT, where he pursues high impact research and development in computer science. He leads several small research groups that focus on some of the core areas, including networking (QoS routing, TCP/IP congestion), distributed systems (performance, security, mobility, reliability), and distributed applications (SCADA, Web/Internet applications, mobile applications). He regularly publishes in prestigious journals like the IEEE Transactions on Parallel and Distributed Systems, IEEE Transactions on Web Services, ACM Transactions on Databases, and conferences ICDCS, WWW, ICSOC etc. He has coauthored two books (John Wiley) and edited more than 10 books. He has been program committee chair of several international conferences, including DOA (Distributed Object and Application Symposium), IFIP DS 11.3 on Database Security, and IFIP 2.6 on Data Semantics. He has also been general chair of more than 12 conferences. He is the recipient of ARC (Australian Research Council) Discovery and Linkage grants and one ARC infrastructure (LIEF) grant (over ½ million).
Mateo Valero is a professor in the Computer Architecture Department at UPC in Barcelona. His research interests focus on high performance architectures. He has published approximately 500 papers, has served in the organization of more than 200 International Conferences, and has given more than 300 invited talks. He is the director of the Barcelona Supercomputing Centre, the National Centre of Supercomputing in Spain. He has been honored with several awards, among them the Eckert-Mauchly Award, the Harry Goode Award, the “King Jaime I” in research, and two national awards on Informatics and on Engineering. He has been named an Honorary Doctor by the University of Chalmers, by the University of Belgrade, by the Universities of Las Palmas de Gran Canaria and Zaragoza in Spain, and by the University of Veracruz in Mexico. He is a “Hall of the Fame” member of the IST European Program (selected as one of the 25 most influential European researchers in IT during the period 1983-2008; Lyon, November 2008). In December 1994, he became a founding member of the Royal Spanish Academy of Engineering. In 2005 he was elected a Correspondant Academic of the Spanish Royal Academy of Science, in 2006 a member of the Royal Spanish Academy of Doctors, and in 2008 a member of the Academia Europaea. He is a fellow of the IEEE, fellow of the ACM, and an Intel Distinguished Research Fellow. More information about him can be found at http://personals.ac.upc.edu/mateo/.

Julio Villalba-Moreno received the BS degree in physics sciences in 1986 from the University of Granada and the PhD degree in computer science in 1995 from the University of Malaga, Spain. From mid 1986 to late 1991 he worked as a design engineer in the Development and Research Department of Fujitsu Spain (D&R Digital Signal Processor group). From late 1986 to 1993 he was an assistant professor, from 1993 to 2007 he was an associate professor. Since 2007 he has been a full professor, all in the Department of Computer Architecture at the University of Malaga. He was a visiting scholar in the Department of Electrical Engineering and Computer Science of the University of California, Irvine in 1996, 2003, 2004, and 2005 for a total of one year. During these stays he did research in computer arithmetic algorithms in collaboration with Professor Tomas Lang. Since 2006, he has been an active member of the program committee of the IEEE International Symposium on Computer Arithmetic. He also belongs to the IEEE-1788 working group Standardization of Interval Arithmetic. Apart from the symposium, he has revised many papers for the IEEE Transactions on Computers and other IEEE journals and conferences. He is the leader of the group “application specific architectures and computer arithmetic” in the Department of Computer Architecture.