The first five months of 2007 have been an exciting time for the *IEEE Transactions on Computers*. Changes in technology and editorial operations have had a significant impact on the IEEE TC community. By its own nature, the *IEEE Transactions on Computers* has been serving an expanding audience by promoting innovations on all fronts. In this respect, as most of you are already aware, the IEEE Computer Society has moved the editorial portal of Manuscript Central to a new version that provides our editorial staff and volunteers with an enhanced set of capabilities to better serve authors and reviewers. All records have been migrated to the latest version of Manuscript Central, so no additional delay will be encountered in the review process of your manuscripts as result of this upgrade.

Also, I would like to remind all authors that a new format is now required for submitting a paper; this is the two-column format that is compatible with the editorial production of TC. This change offers two significant advantages: It allows an accepted paper to be published (either in hard copy or electronically in the IEEE Xplore database) at a fast pace and allows authors to have a better estimate for the length of their article throughout the review process. I invite you to visit the IEEE TC Web page to ensure full compatibility of your manuscript with the new format.

In publication-related activities, during this period, many proposals for Special Sections have been received. I greatly appreciate the fact that distinguished researchers from all over the world have agreed to serve as Guest Editors. For a Special Section, acceptance of articles is very competitive due to the enhanced visibility and specific focus that such an issue provides. This brings noticeable recognition: As TC expands its technical horizon over a diverse set of topics covered, interdisciplinary manuscripts are also being submitted in larger numbers. If you are a potential contributor, please refer to the last pages of different issues of TC for the Call-For-Papers announcement describing in detail the scope and theme of a planned Special Section or check the TC page at www.computer.org.

As an EIC, the coordination of the Editorial Board is certainly an exciting responsibility that touches the core of our community. I would like to take this opportunity to thank the following Associate Editors (AEs) whose terms have recently expired: S. Kundu, B. Mangione-Smith, C.A. Moritz, M. Atallah, A. Rosenberg, M. Dubois, P. Mehra, G. Silberman, N. Nagerzadeh, L. Schwiebert, M. Singhal, A. Tripathi, L. Welch, and Y. Yi. These outstanding professionals have provided unselfish and dedicated service that both the authors and I have appreciated to the fullest extent. Their collegiality and help will be surely missed by all of us.

As the *IEEE Transactions on Computers* continues its long-standing tradition of excellence, it is also my pleasure to introduce the following distinguished colleagues as new Associates Editors: E. Antelo, J.K. Antonio, S. Dolev, T. El-Ghazawi, A.D. George, D. Gizopoulos, J.C. Hou, A. Lysyanskaya, W. Najjar, S. Nikoletseas, J. Vetter, Y.-M. Wang, Y. Yang, M. Yousif, and A.Y. Zomaya. These new AEs have disparate interests to better coordinate new and existing research areas covered by *IEEE TC*; in accordance with an expanding outreach, they are from leading industrial corporations and government laboratories in addition to the traditional supply of academics. They represent the very best and I look forward to working closely with them on an assortment of endeavors. Please refer to their biographical notes at the end of this message to read about their expertise and backgrounds.

Finally, I would like to introduce the new Associate Editor-In-Chief (AEIC) of *IEEE TC*. After a comprehensive evaluation of many potential candidates and with unanimous endorsement of the IEEE CS Publication Board, it is my distinct honor to appoint Professor Cecilia Metra of the University of Bologna as the new AEIC of *IEEE TC*. She will assist me in handling papers that have encountered significant delay in the review process as well as in operational matters (such as appeals) that significantly impact authors. She has significant experience in IEEE-sponsored activities, including the transactions review process and the management of conferences/symposia. As a member of the Editorial Board of *IEEE TC*, she has been among one of the best AEs in terms of responsiveness and fast review time. She is a valuable addition to the TC team; again, her biographical sketch is enclosed.

At *IEEE TC*, we meet the highest standards for a peer-reviewed publication and I thank you for selecting TC as the venue for disseminating your research. As always, do not hesitate to contact me if I can be of help.

Fabrizio Lombardi
Editor-in-Chief

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Cecilia Metra received the degree (summa cum laude) in electronic engineering and the PhD degree in electronic engineering and computer science from the University of Bologna, Italy, where she is now an associate professor in electronics in the Department of Electronic, Computer Science and Systems (DEIS). She is also affiliated with the Advanced Research Center on Electronic Systems for Information and Communication Technologies E. De Castro (ARCES) of the University of Bologna. She was a visiting scholar at the University of Washington, Seattle from 1998 to 2001 and a visiting faculty consultant for Intel Corporation, Santa Clara, California, in 2002. She was general cochair of the IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (2005 and 1999), the IEEE International On-Line Testing Symposium (2006), and the IEEE International On-Line Testing Workshop (2001). She was program cochair of the IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (1998), the IEEE International On-Line Testing Symposium (2005, 2004, and 2003), and the IEEE International On-Line Testing Workshop (2002). She serves/served as topic chair for several international conferences, including the International Test Conference (ITC), the Design, Automation and Test in Europe Conference (DATE), and the IEEE European Test Symposium (ETS), and as a member of the Organizing Committee and/or Technical Program Committee of several international conferences, including the Design Automation Conference (DAC), the IEEE VLSI Test Symposium (VTS), the IEEE International Workshop on Design for Manufacturability & Yield, the IEEE International Workshop on Infrastructure IP, and the IEEE International Workshop on Silicon Debug and Diagnosis. She received two IEEE Computer Society Certificates of Appreciation (in 2000 and 2004) and an IEEE Computer Society Meritorious Service Award (in 2006). She has served as a guest editor of special issues in archival journals and magazines such as the IEEE Transactions on Computers, the Journal of Electronic Testing: Theory and Applications, and IEEE Design and Test. Her research interests are in the field of design and test of digital systems, reliable and error-resilient systems, fault tolerance, online testing, fault modeling, concurrent diagnosis, debug, emerging technologies, and nano computing.

Elisardo Antelo graduated with a degree in physics in 1991 and received the PhD degree in computer engineering in 1995 from the University of Santiago de Compostela, Spain. In 1992, he joined the Departamento de Electronica e Computacion at the University of Santiago de Compostela. From 1992 to 1998, he was an assistant professor and, since 1998, he has been a tenured associate professor in this department. He was a research visitor at the University of California at Irvine several times between 1996 and 2000. Dr. Antelo is a member of the Computer Architecture Group at the University of Santiago de Compostela. In 1999, he was one of the recipients of a Research Initiation Award from the Xunta de Galicia (local government); in 2001, he received an award from the Xunta de Galicia and the University of Santiago de Compostela for a spin-off project related to the design of intellectual property blocks for numerical computations. Since 2001, he has been involved on the Program Committee of the IEEE Symposium on Computer Arithmetic. He also was involved with the Program Committee of the Seventh Real Numbers and Computers Conference in 2006. His primary research and teaching interests are in digital design and computer architecture, with current emphasis on high-speed and low-power numerical processors, application-specific modules, computer arithmetic, and analytical models for the design of multicore processors. Dr. Antelo is member of the IEEE and the IEEE Computer Society.

John K. Antonio received the BS, MS, and PhD degrees in electrical engineering from Texas A&M University in 1984, 1986, and 1989, respectively. He is a professor of computer science and director of IOTA (Institute for Oklahoma Technology Applications) at the University of Oklahoma. He served as director of the School of Computer Science at the University of Oklahoma from 1999 to 2006. Before joining the University of Oklahoma, he was on the faculty of the Department of Computer Science at Texas Tech University and the faculty of the School of Electrical and Computer Engineering at Purdue University. His research interests include embedded high performance computing, low-power and power-aware computing, reconfigurable computing, computer architecture, and parallel and distributed computing. Dr. Antonio is a senior member of the IEEE.
Shlomi Dolev received the BSc degree in engineering and the BA degree in computer science in 1984 and 1985 and the MSc and DSc degrees in computer science in 1990 and 1992 from the Technion Israel Institute of Technology. From 1992 to 1995, he was with Texas A&M University as a visiting research specialist. In 1995, he joined the Department of Mathematics and Computer Science at Ben-Gurion University. He was a visiting researcher/professor at MIT, DIMACS, and LRI for several periods during summers. He is the author of the book *Self-Stabilization* (MIT Press). He has published more than 100 journal and conference scientific articles and served on the program committees of more than 40 conferences. He is an associate editor of the *AIAA Journal of Aerospace Computing, Information and Communication* and a guest editor of the *Distributed Computing Journal*. He established the Computer Science Department at Ben-Gurion University and served as the first chair of the department, where he is now a full professor holding the Rita Altura Trust Chair in computer science. His current research interests include distributed computing, distributed systems, communication networks, and fault-tolerant hardware and software; in particular, the self-stabilization property of such systems.

Tarek El-Ghazawi received the PhD degree in electrical and computer engineering from New Mexico State University in 1988. He is a professor in the Department of Electrical and Computer Engineering at George Washington University. He is the director of the GWU Institute for Massively Parallel Applications and Computing Technology (IMPACT) and a codirector of the US National Science Foundation Industry/University Center for High-Performance Reconfigurable Computing (CHREC). Dr. El-Ghazawi’s research interests include high-performance computing, computer architectures, reconfigurable computing, embedded computing, and applications to remote sensing and image processing. He is one of the principal coauthors of the UPC parallel programming language. He has authored/coauthored one book, several book chapters, and more than 150 refereed research publications. He received the IBM faculty award in 2004 and has been serving as a consultant and on the technical/science advisory boards for many government and industrial organizations. He is a senior member of the IEEE and a member of the ACM, IFIP WG 10.3, and the Phi Kappa Phi National Honor Society.

Alan D. George received the BS degree in computer science and the MS degree in electrical and computer engineering from Florida State University in 1982, 1985, and 1991, respectively. He is a professor of electrical and computer engineering at the University of Florida, the flagship university in the fourth most-populous state in the US. He serves as director of the High-performance Computing and Simulation (HCS) Research Laboratory, chair of the University Committee on High-Performance Computing, and director of a new US National Science Foundation Research Center, the NSF Center for High-Performance Reconfigurable Computing (CHREC). CHREC is both a center and a consortium, with four university partners and more than a dozen federal and industry partners. Prior to pursuing a career in academia, he served as a senior computer engineer and group leader at Martin Marietta (now Lockheed Martin) and at General Electric. Professor George’s research interests focus on high-performance architectures, networks, services, systems, and applications for reconfigurable, parallel, distributed, and fault-tolerant computing. He is a senior member of IEEE and SCS and a member of the ACM and AIAA.

Dimitris Gizopoulos received the engineering diploma from the Computer Engineering and Informatics Department at the University of Patras (1992) and the PhD degree from the Department of Informatics and Telecommunications at the University of Athens (1997). In 1999, he joined the Department of Informatics, University of Piraeus, Greece, as a lecturer and is now serving the same department as an assistant professor. His research interests include microprocessors and microprocessor-based systems design, test and fault tolerance, embedded systems design, test, and reliability, as well as fault modeling, self-testing, and online testing of digital computing systems. He has published more than 75 papers in peer reviewed transactions, journals, and conference proceedings, is co-inventor of a US patent, author of a book, and editor of a second in Springer’s Frontiers in Electronic Testing book series. He is an associate editor of *IEEE Design and Test of Computers* and Springer’s *Journal of Electronic Testing: Theory and Applications*, as well as a guest editor for several Special Issues (*IEEE Transactions on VLSI Systems, IEEE Design and Test of Computers*, and *IEEE Communications Magazine*). He is involved in the organization and technical programs of many international conferences. Since 2004, he has been a member of the Steering Committee of the IEEE International Test Conference (ITC). He is program chair of the IEEE International On-Line Testing Symposium (2007) and, since 2003, the program chair of the IEEE Workshop on Infrastructure IP. He is a member of the Executive Committee of the IEEE Computer Society Test Technology Technical Council (TTTC), with contributions to the Technical Meetings and the Tutorials and Education Groups. He is a senior member of the IEEE and a Golden Core Member of the IEEE Computer Society.
Jennifer C. Hou received the BSE degree in electrical engineering from National Taiwan University in 1987, the MSE degrees in electrical engineering and computer science and in information and operations engineering from the University of Michigan, Ann Arbor, in 1989 and in 1991, and the PhD degree in electrical engineering and computer science, also from University of Michigan, Ann Arbor, in 1993. She was an assistant professor in the Electrical and Computer Engineering Department at the University of Wisconsin-Madison from 1993-1996 and an assistant/associate professor in electrical engineering at Ohio State University, Columbus, from 1996-2001. Since August 2001, she has been with the Department of Computer Science at the University of Illinois at Urbana Champaign, where she is currently a professor. Dr. Hou has been supervising several federally and industry funded projects in the areas of network modeling and simulation, network measurement and diagnostics, enabling software infrastructure for assisted living, and both the theoretical and protocol design aspects of wireless sensor networks. She has published (with her former advisor, students, and colleagues) more than 150 papers in archived journals, book chapters, and peer-reviewed conferences, and released an extensible, reusable, component-based, compositional network simulation and emulation package, J-Sim. She has been involved in organizing several international conferences sponsored by professional organizations, such as ACM Mobicom, IEEE INFOCOM, IEEE MASS, and IEEE RTAS, as well as being an editor for archival journals and magazines such as the IEEE Transactions on Wireless Communications, IEEE Transactions on Parallel and Distributed Systems, IEEE Wireless Communication Magazine, Kluwer Computer Networks, and ACM Transactions on Sensor Networks. She was a recipient of an ACM Recognition of Service Award in 2004, a Cisco University Research Award from Cisco, Inc., in 2002, a Lumley Research Award from Ohio State University in 2001, a US National Science Foundation CAREER award from the Network and Communications Research Infrastructure, National Science Foundation in 1996-2000, and a Women in Science Initiative Award from the University of Wisconsin-Madison in 1993-1995. She is a senior member of the IEEE and a member of the ACM.

Anna Lysyanskaya received the AB degree in computer science and mathematics from Smith College in 1997 and the PhD degree in computer science and electrical engineering from the Massachusetts Institute of Technology in 2002. She is an assistant professor of computer science at Brown University. She is a recipient of the US National Science Foundation CAREER award. Her research interests are in cryptography, theoretical computer science, and computer security.

Walid Najjar received the BE degree in electrical engineering from the American University of Beirut in 1979 and the MS and PhD degrees in computer engineering from the University of Southern California (USC) in 1985 and 1988, respectively. From 1986 to 1989, he was with the USC-Information Sciences Institute. From 1989 to 2000, he was on the faculty of the Department of Computer Science at Colorado State University. He joined the Department of Computer Science and Engineering at the University of California Riverside in 2000. Dr. Najjar is an associate editor of the IEEE Computer Architecture Letters and the Elsevier Journal of Parallel Computing. He has been involved in the technical program committees and organization of a number of professional conferences, including HPCA, MICRO, CASES, ISSS+CODES, DATE, FPL, and PACT. His research interests are in the fields of computer architecture and compiler optimizations, embedded systems, and sensor networks. Lately, he has been very active in the area of compilation for FPGA-based code acceleration and reconfigurable computing. His research has been supported by the NSF, DARPA, and various industry sponsors.
Sotiris Nikoletseas is currently an assistant professor in the Computer Engineering and Informatics Department at Patras University, Greece. He is also a senior researcher and director of the SensorsLab at the Research Academic Computer Technology Institute, Greece. His research interests include algorithmic techniques in distributed computing (with a focus on wireless sensor networks and ad hoc mobile networks), fundamental aspects of modern networks (focus on network reliability), probabilistic techniques and random graphs, average case analysis of algorithms, computational complexity and approximation algorithms, algorithmic engineering, and large-scale simulation. He has coauthored more than 100 publications in international journals and refereed conferences, several invited chapters in books by major publishers, and a book on the probabilistic method. He has served as the Program Committee chair for many conferences (including ALGOSENSORS, MSWIM, MOBIWAC, WMAN, WEA), and as an editor of Special Issues and member of the editorial boards of major journals (such as TCS, JEA, and IJDSN). He has co-initiated several international events (including ALGOSENSORS and DCOSS). He has delivered several invited talks and tutorials. He has participated in/coordinated several externally funded European Union R&D Projects related to fundamental aspects of modern networks.

Jeffrey Vetter received the PhD degree in computer science from the Georgia Institute of Technology. He is a computer scientist in the Computer Science and Mathematics Division (CSM) of Oak Ridge National Laboratory (ORNL), where he leads the Future Technologies Group and directs the Experimental Computing Laboratory. Dr. Vetter is also a joint professor in the College of Computing at the Georgia Institute of Technology. His research interests target the areas of experimental software systems and architectures for high-end computing. His interests span several areas of experimental systems for high-end computing (HEC)—encompassing architectures, system software, and tools for performance and correctness analysis of applications. Professionally, he has published more than 70 papers, served on more than 30 program committees, and served as the area chair for HEC performance at three major conferences. His papers have won awards at the International Parallel and Distributed Processing Symposium and EuroPar. The coherent thread through his research is developing rich architectures and software systems that solve real-world HEC problems. In some cases, his efforts have provided an understanding of an application’s fitness for a specific architecture, such as his characterizations of several important HEC benchmarks with his Sequoia toolkit. In other cases, his effort provided a new system intended to aid in the understanding and interpretation of a performance or correctness condition, such as his work on the scalable MPI performance analysis tools using multivariate statistics and machine learning. Currently, his research addresses problems in analyzing new architectures for HEC systems using performance measurement, modeling, and simulation. In particular, he has been investigating the effectiveness of next-generation architectures, such as massively multithreaded processors, vector processors, heterogeneous multicores processors, and field-programmable gate arrays (FPGAs), for strategic applications.

Yi-Min Wang graduated in 1986 from National Taiwan University with the BS degree in electrical engineering and the top-of-the-class honor. In 1988, he joined the Electrical and Computer Engineering Department at the University of Illinois at Urbana-Champaign, where he received the master’s degree in 1990 and the PhD degree and the Robert T. Chen Memorial Award for excellence in research in 1993. He is currently a principal researcher at Microsoft Research, Redmond, Washington. He was responsible for founding the Cybersecurity and Systems Management Research Group to focus on developing unconventional scientific solutions to big, real-world problems. Several key technologies his group developed under the “Strider” umbrella project have made their way into Microsoft products and services. He has received the selective Microsoft Gold Star Award several times for his contributions and is the holder of 23 US patents. Prior to joining Microsoft, Dr. Wang was a principal technical staff member at AT&T Research, focusing on reliable distributed systems. He was most well-known for his research work on checkpointing, both in theory and in practice. He has been involved in organizing many international symposia and conferences, including serving as a program cochair of the 2005 International Conference on Autonomic Computing (ICAC), the program vice-chair of the Fault-Tolerant and Dependable Computing Track of the 2005 International Conference on Distributed Computing Systems (ICDCS), and a program committee member of the International Conference on Dependable Systems and Networks (DSN), ACM Symposium on Principles of Distributed Computing (PODC), International World Wide Web Conference (WWW), and the USENIX Security Symposium. His research interests are Internet security, systems management, reliability, fault tolerance, distributed systems, software systems, operating systems, and networking.
Yuanyuan Yang received the PhD degree in computer science from the Johns Hopkins University, Baltimore, Maryland, in 1992. She is currently a professor of electrical and computer engineering and computer science at the State University of New York (SUNY) at Stony Brook, where she also directs the High-Performance Computing and Networking Research Laboratory. Her research interests include interconnection networks, wireless/mobile networks, optical networks, high-speed networks, multicast communication, and parallel and distributed computing systems. She has authored or coauthored more than 160 research articles in leading refereed journals and conferences with about 40 papers published in various IEEE transactions on these topics. She is also an inventor/co-inventor of six US patents in the area of interconnection networks. Dr. Yang served as an associate editor for the IEEE Transactions on Parallel and Distributed Systems from 2001-2005 and is currently a subject area editor for the Journal of Parallel and Distributed Computing. She has served as a distinguished visitor of the IEEE Computer Society. She received an IEEE Region 1 Award for “significant contributions in multicast switching networks” in 2002 and a Best Paper Award on optical interconnects at the 18th IEEE International Parallel and Distributed Processing Symposium (IPDPS) in 2004. She has served as a general chair, program chair, or vice chair for several major conferences and a program committee member for numerous conferences. More information about her and her research can be found at http://www.ece.sunysb.edu/~yang.

Mazin Yousif received the master’s and PhD degrees from the Pennsylvania State University in 1987 and 1992, respectively. He is a principal engineer in the Corporate Technology Group at Intel Corporation in Hillsboro, Oregon. He currently leads a team focusing on platform provisioning and virtualization to enable platform autonomies and Capacity on Demand (CoD) in scale-out environments. Prior to that, he worked on InfiniBand and datacenter I/O interconnects. During his involvement with the InfiniBand Architecture, he cochaired the InfiniBand Trade Association (IBTA) Management Working Group. From 1993 to 1995, he was an assistant professor in the Computer Science Department at Louisiana Tech University. He worked for IBM’s xSeries Server Division in Research Triangle Park (RTP), North Carolina, from 1995-2000. He has served as an adjunct professor at various universities including the Oregon Graduate Institute (OGI), Duke, and North Carolina State. His research interests include computer architecture, clusters and grid computing, autonomic computing, workload characterization, and performance evaluation. He has published more than 50 articles in his areas of research. He chaired the program committees of several conferences/workshops and has been on the program committees of many others. He is on the advisory board of the Journal of Pervasive Computing and Communications (JPCC) and is an editor for Cluster Computing and the Journal of Networks, Software Tools and Applications. He is a senior member of the IEEE.

Albert Y. Zomaya is currently the Head of School and the CISCO Systems Chair Professor of Internetworking in the School of Information Technologies at the University of Sydney, Australia. Prior to joining Sydney University, he was a full professor in the Electrical and Electronic Engineering Department at the University of Western Australia, where he also led the Parallel Computing Research Laboratory during the period 1990-2002. He served as associate, deputy, and acting head of the same department and held visiting positions at Waterloo University, Canada, and the University of Missouri-Rolla. He is the author/coauthor of six books, more than 200 publications in technical journals and conferences, and the editor of seven books and seven conference volumes. He is currently an associate editor for 14 journals, the founding editor of the Wiley Book Series on Parallel and Distributed Computing, and a founding coeditor of the Wiley Book Series on Bioinformatics. Professor Zomaya was the chair the IEEE Technical Committee on Parallel Processing (1999-2003) and currently serves on its executive committee. He has been actively involved in the organization of national and international conferences. He received the 1997 Edgeworth David Medal from the Royal Society of New South Wales for outstanding contributions to Australian Science. In September 2000, he was awarded the IEEE Computer Society’s Meritorious Service Award. He is a chartered engineer (CEng), a fellow of the IEEE, a fellow of the Institution of Electrical Engineers (United Kingdom), and a member of the ACM. His research interests are in the areas of high performance computing, parallel algorithms, mobile computing, and bioinformatics.