1) As one goes through the literature on fault-tolerant processor arrays, one often finds that apparently comparable papers are, in fact, solving distinct problems, although such is not obvious from the presentation. The distinction made by Professor Koren between manufacturing defects and operational faults is indeed a valid one. Had I recognized that he was dealing with the latter, I would never have voiced an opinion on the suitability of his techniques for the former.

2) Professor Koren points out that my paper concentrates on fault-tolerant realizations of only three families of graphs. This fact reflects both my state of knowledge at the time and my approach to fault-tolerant array design: On the one hand, one can seek efficient fault-tolerant realizations for individual graph families. Alternatively, one can find an efficient fault-tolerant realization for one single "master" family (such as rectangular grids) and induce fault tolerance in other families via embeddings into this master family. There is no consensus on which approach is to be preferred; there are respected researchers who have opted in each direction; I have opted for the former approach. Although the subject paper deals only with linear arrays, trees, and pyramids, subsequent work by F. R. K. Chung, F. T. Leighton, and me [1], [2] extends the DIOGENES technique to arbitrary graphs.

3) Regarding the observed vulnerability of the buses and switches in DIOGENES layouts: a) such vulnerability is a weakness of all solution approaches that attain fault tolerance by realizing interconnections through an external switching network. b) colleagues in the processing area have assured me that simple switching networks such as those used in DIOGENES designs can be made so reliable that they can in fact be deemed invulnerable to faults. c) I must turn this issue around to Professor Koren and ask him how his solution techniques will work if the pass-through capability of a processing element fails when the element does. I am sure that he, just as I, will have to be satisfied with the assurance that conservative fabrication can render such total failure *very* unlikely.

References

[1] F. R. K. Chung, F. T. Leighton, and A. L. Rosenberg, "DIOGENES—A methodology for designing fault-tolerant VLSI processor arrays," in *Proc. 13th Int. Conf. Fault-Tolerant Computing*, 1983, pp. 26–32.

[2] ——, "Embedding graphs in books: A layout problem with applications to VLSI design," submitted for publication, 1984.

Correction to "Fault-Tolerant Multiprocessor Link and Bus Architectures"

D. K. PRADHAN

In the above paper[1] the following typographical errors should be corrected.

Page 36: The definition of the path $pt(s, d)$ should be corrected as follows;

$$
\begin{aligned}
&(s_{m-1}, \cdots\cdots\cdots, s_1 s_0)\\
&(s_{m-1}, \cdots\cdots\cdots, s_1, d_{m-1})\\
&(s_{m-2}, \cdots, s_1, d_{m-1}, s_{m-1})\\
&(s_{m-2}, \cdots, s_1, d_{m-1}, d_{m-2})\\
&\quad\vdots\\
&(s_1, d_{m-1}, d_{m-2}, \cdots\cdots, s_2)\\
&(s_1, d_{m-1}, d_{m-2}, \cdots\cdots, d_1)\\
&(d_{m-1}, \cdots\cdots\cdots, d_1, s_1)\\
&(d_{m-1}, \cdots\cdots\cdots, d_1, d_0)
\end{aligned}
$$

Page 40 Lemma 3: $x \neq yy$ should be changed to $x \neq y$.

Page 41: uk in Lemma 7 should read yk.

Page 41: Consider the following $(r \cdot 2)$ paths should be changed to $(r - 2)$ paths. In Theorem 8 the path length should be changed to $(6m - 1)$ (Since according to case III, fault-free path from xk to yk is of length at most $(2m + 1)$ instead of $(2m - 1)$.

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[1] D. K. Pradhan, *IEEE Trans. Comput.*, vol. C-34, pp. 33–45, Jan., 1985.