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This index covers all items—papers, correspondence, reviews, etc.—that appeared in this periodical during 1982, and items from prior years that were commented upon or corrected in 1982. The index is divided into an Author Index and a Subject Index, both arranged alphabetically.

The Author Index contains the primary entry for each item; this entry is listed under the name of the first author and includes coauthor names, title, location of the item, and notice of corrections and comments if any. Cross-references are given from each coauthor name to the name of the corresponding first author. The location of the item is specified by the journal name (abbreviated), year, month, and inclusive pages.

The Subject Index contains several entries for each item, each consisting of a subject heading, modifying phrase(s), first author's name—followed by + if the paper has coauthors—and enough information to locate the item. For coauthors, title, comments, and corrections if any, etc., it is necessary to refer to the primary entry in the Author Index. Subject cross-references are provided as required by the subject matter. Also provided whenever appropriate are listings under generic headings such as Bibliographies (for any paper with at least 50 references, as well as papers that are exclusively bibliographies), Book reviews, and Special issues.

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Image reconstruction
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Image region analysis
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Industrial control
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Industrial power system transients
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Information systems
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Information theory
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Integrated circuits
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Integrated circuits; cf. Digital integrated circuits; MOS integrated circuits; Semiconductor logic circuits; Semiconductor memories

Integrated-circuit fabrication; cf. Layout
Integrated-circuit interconnections; cf. Integrated-circuit metallization; Layout

Integrated-circuit measurements; cf. Integrated-circuit testing

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Integrated-circuit metallization
computer random logic; relation between partitioning properties of computer logics and distribution of connection lengths. Feuer, Michael, T-C Jan 82 29-33
VLSI yield model with module redundancy; effects of interconnect densities and logic module complexities. Mangir, Tulin Erdim, +, T-C Jul 82 609-616

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Interconnected systems; cf. Hierarchical systems
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Logic; cf. Specific topic
Logic arrays
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Logic circuit fault tolerance
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Logic circuit testing; cf. Asynchronous sequential logic circuit testing; Combinational logic circuit testing; Sequential logic circuit testing
Logic circuits; cf. Combinational logic circuits; Counting circuits; Flip-flops; Logic arrays; Logic modules; Semiconductor logic circuits; Sequential logic circuits; Stochastic logic circuits
Logic design
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Logic design; cf. Logic modules
Logic functions
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Logic modules
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VLSI (large-scale integration); cf. Integrated circuits

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Magnetic bubble memories
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Matrices
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Matrix multiplication
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Memories
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Memories; cf. Associative memories; Cache memories; Paged memories; Semiconductor memories
Memory allocation; cf. Memory management
Memory fault tolerance
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Memory management
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Memory testing
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Microcomputer software; cf. Specific application

Microprocessors

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Microprocessors; cf. Microcomputer networks; Multiprocessing

Microprogramming

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Military computers

real-time systems; modular approach using very high speed integrated circuit technology. Arnold, Robert G., +, T-C May 82'385–398

Missile computers

real-time systems; modular approach using very high speed integrated circuit technology. Arnold, Robert G., +, T-C May 82'385–398

MOS

abbr. Metal-oxide-semiconductor.

MOS integrated circuits, logic

large MOS combinational networks designed for testability; testing. El-Zay, Yacoub M., +, T-C Feb 82'129–139


MOS integrated circuits, logic; cf. CMOS; integrated circuit, logic

MOS/CMOS circuits

Motion measurement; cf. Image motion analysis

Multidimensional signal processing; cf. Image processing

Multilevel systems; cf. Hierarchical systems

Multiplication

canonical bit-serial multiplier suitable for VLSI implementation. Strader, Joel R., +, T-C Aug 82'791–795

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HMIP hierarchical multiprocessor; tree-structured multiprocessor having two distinct hierarchies for data processing and data distribution. Shin, Kang S., +, T-C Nov 82'1045–1053

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MP/C multiprocessor/computer architecture for concurrent computing. Arden, Bruce W., +, T-C May 82'455–473

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Multiprocessing; cf. Distributed computing; Microcomputer networks

Parallel processing

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SIMD machines with Augmented Data Manipulator interconnection network; number of distinct data permutations performable in single pass through ADM network. Adams, George B., III, +, T-C Apr 82'270–277

Multivibrators; cf. Flip-flops

Parallel processing

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Nets; cf. Petri nets

Networks; cf. Circuits; Computer communication

Nonrecursive digital filters

cf. Digital filter, Approximation; P-level maximal-length sequences; autocorrelation function. Westman, Gerhard, T-C Jan 82'75–77

Numerical methods; cf. Arithmetic; Matrices; Partial differential equations

O

Office automation


Operating systems; cf. Computer software, operating systems

Optimization methods; cf. Dynamic programming

Orthogonal transforms; cf. Transforms

P

Parallel processing

algorithm for solution of triangular systems on parallel processing system. Montoye, Robert K., +, T-C Nov 82'1076–1082

bit-serial parallel processing systems; airborne associative processor and ground-based massively parallel processor. Batchter, Kenneth E., T-C May 82'377–384

Burroughs Scientific Processor; BSP; high-performance scientific computer combining parallelism and pipelining with conflict-free access to arrays in parallel memory. Kuck, David J., +, T-C May 82'363–376

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ETH-multiprocessor EMPRESS; dynamically configurable multiple-instruction stream–multiple-data stream-capable of handling two-stage parallelism. Buehrer, Richard E., +, T-C Nov 82 1035–1044

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Fortran-like loops; improved time and parallel processor bounds. Heult, Richard W., +, T-Jan 78–81

general-purpose high-speed, parallel image transform image processor. Herron, J. M., +, T-C Aug 82 795–800

generalized parallel counter synthesized from network of smaller ones; upper bound to number of levels required. Dormido, S., +, T-C Aug 82 699–705

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large linear equation systems; elimination-tree as data structure for parallel L/U decomposition. Joss, Jochen A. G., +, T-C Mar 82 231–239


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(0) parallel multiplier with bit-sequential input and output. Sips, H. J., T-C Apr 82 325–327

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wavefront-based language and architecture for programmable special-purpose VLSI multiprocessor array. Kang, Sun-Tuan, +, T-C Nov 82 1054–1066

Parallel processing; cf. Computer pipeline processing; Multiprocessing

Partial differential equations
parallel solution of partial differential equations on distributed computing system. Oelenbe, Erol, +, T-Dec 82 1157–1164

Pattern classification
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Pattern clustering methods
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Pattern recognition
regular expression compiler for custom VLSI layout; implementation of recognizers using networks of programmable logic arrays. Trickey, Howard W., T-C Jun 82 514–520

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Pattern recognition; cf. Image analysis; Pattern classification

Perturbation networks
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Bench perturbation network, parallel algorithm to determine switch setting. Nassimi, David, +, T-C Feb 82 148–154

matrix decomposition algorithm for perturbation networks. Kabale, Marek, T-C Mar 82 265

SIMD machines with Augmented Data Manipulator interconnection network, number of distinct data permutations performable in single pass through ADM network. Adams, George B., III, +, T-C Apr 82 270–277

Permutation
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Petri nets
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Picture processing; cf. Image processing

Pipeline processing; cf. Computer pipeline processing

Power supplies; cf. Computer power supplies

Probability
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Programmable control
programmable digital signal processors; architecture of Bell Laboratories' Synchronous Distributed Processor. Shively, Richard R., T-C Jan 82 16–22

Programming; cf. Computer languages; Microcomputer software; Specific application

Pseudorandom sequences; cf. Shift-register sequences

Pulse analysis; cf. Electromagnetic transient analysis

Q

Queueing analysis
computer performance models of parallel processing systems in which job subdivisions into two or more asynchronous tasks; queueing network models. Heidelberger, Philip, +, T-C Nov 82 1099–1109

R

Rail transportation
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Random ...; cf. Probability; Stochastic ...

Random number generation; cf. Pseudorandom number generation

Recurrent coding; cf. Convolutional coding

Reed–Solomon coding
symbol-sliced logic structure for VLSI implementation of Reed–Solomon encoders. Liu, Kang Y., T-C Feb 82 170–175

Registers; cf. Register setting

Relaxation oscillators; cf. Flip-flops

Reliability; cf. System reliability

Residue arithmetic
autocolline residue multiplier which inhibits dynamic range overflow. Taylor, Fred J., +, T-C Apr 82 321–325

residue arithmetic multipliers that overcome moduli size limitation by using VLSI technology, special architectures, and moduli choice. Taylor, Fred J., T-C Jun 82 540–546

Roundoff errors; cf. Finite wordlength effects

S

Sampling methods; cf. Signal sampling/reconstruction

Space computers; cf. Space-vehicle computers

Search methods; cf. Database systems, searching; Information systems

Semiconductor device testing; cf. Integrated-circuit testing

Semiconductor logic circuits
computer random logic; relation between partitioning properties of computer logic and distribution of connection lengths. Feuer, Michael, T-C Jan 82 29–33

VLSI yield model with module redundancy; effects of interconnect densities and logic module complexities. Mangir, Titila Erdin, +, T-C Jul 82 609–616

Semiconductor logic circuits; cf. CMOS integrated circuits, logic; Logic circuit testing; MOS integrated circuits, logic

Semiconductor memories
reliability of memory with single-error correction. Mikhail, W. F., +, T-C Jun 82 560–564

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single-byte error correcting – double-byte error detecting codes for increased memory reliability. Kaneda, Shigeo, +, T-C Jul 82 596–602

Sequences; cf. Shift-register sequences

Sequential logic circuit testing
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Sequential logic circuit testing; cf. Asynchronous sequential logic circuit testing

Sequential logic circuits
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Sequential logic circuits; cf. Asynchronous sequential logic circuits; Automata

Shift-register sequences
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Signal processing
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systolic processing of signals and images; VLSI implementation. Kulkarni, Ashok V., +, T-C Oct 82 1000–1009

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Signal processing; cf. Image processing

Signal sampling/reconstruction; cf. Image reconstruction

Site security monitoring
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Software; cf. Computer software

Sorting/merging
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Source coding; cf. Arithmetic coding

Space-vehicle computers
real-time supervisories; modular approach using very high speed integrated circuit technology. Arnold, Robert G., +, T-C May 82 385–398

Special issues
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reliable and fault-tolerant computing. T-C Jul 82 575–706

supervisories; current state-of-the-art. T-C May 82 345–473

Square-rooting
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Stochastic automata
optimal illumination region algorithm for convex polygons. Lee, Der-Tsai, +, T-C Dec 82 1225–1227

Stochastic logic circuits
computer random logic; relation between partitioning properties of computer logic and distribution of connection lengths. Feuer, Michael, T-C Jan 82 29–33

Stochastic processes; cf. Markov processes

Storage; cf. Memories

Store-and-forward switching; cf. Message switching

Supervisories; cf. Distributed computing; Parallel processing

Switching circuits; cf. Semiconductor logic circuits

Switching functions; cf. Logic functions

Switching systems; cf. Interconnection networks

System reliability; cf. Computer reliability; Computer software reliability; Fault tolerance

Terrain mapping
entity-oriented relational database system for spatial information; application to watershed data. Vaidya, Prashant D., +, T-C Oct 82 1025–1031

Testing; cf. Computer software testing; Computer testing; Digital system testing

Text processing
hardware-based hashing scheme in design of multiliterm string comparator for text retrieval. Burkowski, Forben J., T-C Sep 82 825–834

Time synchronization; cf. Synchronization

Tomography, X-ray
supersystem technology and architecture. Swartzlander, Earl E., Jr., +, T-C May 82 399–409

Transforms
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two-dimensional discrete cosine transform; fast algorithms. Kamangar, F., +, T-C Sep 82 899–906

Transforms; cf. Haar transform

Transient analysis; cf. Electromagnetic transient analysis

Trees
error correction in robust data structures. Taylor, David J., +, T-C Jul 82 602–608

image region-labeling and clustering problems; parallel solution using content-addressable read/write memories suitable for VLSI implementation. Snyder, Wesley E., +, T-C Oct 82 963–968

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point enclosure problem; solution in plane using S-tree static data structure. Vaishnavi, Vijay K., T-C Jan 82 22–29

Trees; cf. Hierarchical systems

Truncation errors; cf. Finite wordlength effects

V

Vehicle control; cf. Aircraft control

VLSI (very large-scale integration); cf. Integrated circuits

W

Water resources
entity-oriented relational database system for spatial information; application to watershed data. Vaidya, Prashant D., +, T-C Oct 82 1025–1031

Wiring; cf. Integrated-circuit metallization; Layout

X

X-ray imaging; cf. Tomography, X-ray

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