sweep rate. Note that the presence of the Schmitt trigger section significantly degrades the synchronization performance of the flip-flop. The circuit of Fig. 1 was also tested by applying a negative-going marginal pulse to the set (S) input, after resetting, and the resulting output was the same as shown in Fig. 4.

The response of the Fig. 2 circuit is shown in Fig. 6. Here again the output can oscillate several times before settling. A TTL Schmitt trigger integrated circuit, the 7413, had been previously tested in a circuit somewhat like Fig. 2 to measure the probability the Schmitt trigger was unresolved as a function of the time waited before sampling the output. The results of testing two packages indicate that 7413 Schmitt triggers in a circuit of the type shown in Fig. 2 will provide performance similar to that provided by cross-tied gates of the 7404 type.

The primary intent of this note is to challenge the belief still held by some logic designers that there is an electrical or logical circuit that will provide the synchronizer function, in a bounded time, with probability zero of a failure to synchronize. There are, of course, ways to improve synchronizer performance, but guarantee resolution in a finite time is not possible. There are circuits that provide a zero failure rate in an unbounded time, but with a short average propagation time, for use in speed-independent, delay-insensitive asynchronous designs [4]-[6]. For clocked systems, a synchronizer design that uses a high-speed tunnel diode as the decision element in an ECL system has been reported to provide very good reliability with only an 11 ns propagation delay [6].

In closing, there is a great deal of theoretical and experimental evidence that a region of anomalous behavior exists for every device that has two stable states. The maturity of this topic is now such that papers making contrary claims without theoretical or experimental support should not be accepted for publication.

Support for T. J. Chaney’s Comments on “A Note on Synchronizer or Interlock Maloperation”

E. GORDON WORMALD

Chaney’s masterful exposition [1] on my suggestion [2] for defeating synchronizer or interlock maloperation should provide some much needed publicity for the nature and possible effects of synchronizer metastability. Hopefully, the discussion will discourage further attempts to eliminate this unavoidable characteristic.

It seems that the classes of action possible to mitigate such maloperation are twofold.

1) Design the hardware to reduce the probability of metastability, as in [3] or [4].

2) Design the software to minimize the ill effects of an occasional maloperation. Apparently there are systems which crash or suffer other major disturbances when the unavoidable occurs [5]. What is required is in effect an error-correcting arrangement embracing the synchronizer and the separately clocked subsystems which are to communicate through it.

Obviously the situation needs understanding by a much wider circle in the computing fraternity than the small proportion of engineers who have been concerned so far.

REFERENCES


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Comments on “Multiple Fault Detection in Combinational Network”

BELLA BOSE

In the above paper, the authors have defined complete test, closed fault set, fault set graph, and undetected fault set as follows.

Definition 2—Complete Test (T): A complete test set detects any single fault in an irredundant network.

Definition 11—Closed Fault Set: A closed fault set is a set of faults such that each element in the set is masked by another element in the set when it is under test.

Definition 12—Fault Set Graph: A fault set graph is a graph with a vertex for each element in a set of multifaults and a directed edge between i and j if fault i masks fault j.

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