A Study of the Electrochemical Cell as a Storage Element for the Memory Access Gap

THOMAS J. NELSON

Abstract—A memory device is proposed which is intended to fill the memory access gap, i.e., whose speed, cost, and capacity are intermediate between those of the electronic and electromechanical memories. Information is stored by electroplating metal on one or the other of two electrodes. The memory is random access and nonvolatile. Selection is by a coincident-voltage technique and stack operation is similar to the operation of core memories. The estimated driving requirement of a selection line is 1 V at 1 mA, indicating that small-area IC logic circuits will be able to drive the memory. The proposed memory will be mass-fabricated and the cost is foreseen as being primarily the interconnection cost between the IC decoding and sensing chips and the bit select conductors. The cost is estimated at 5 mcents/bit.

Measurements of the I–V characteristics, capacitance, switching time, and read discrimination in a single cell indicate that operation with a cycle time of 100 to 200 μs is feasible and consistent with a stack size of 10⁸ bits. The eventual feasibility of the memory will depend on the solution of two main problems: obtaining an adequate selection threshold and eliminating or reducing the reaction of the electrodeposited metal with trace impurities in the electrolyte. Possible ways of attaining these goals are discussed; however, until these goals are achieved the proposed memory must be viewed as speculative. It should be pointed out, however, that based on the state of current electrochemical theory no fundamental reason exists as to why the goals may not be achieved.

Index Terms—Electrochemical memory, electronic bulk memory, memory access gap device, memory hardware.

I. INTRODUCTION

In present-day memory hierarchies there exists a “memory access gap” [1]. This refers to the ratio of approximately 1000 which exists between the access time of the slowest electronic memories (10 μs) and the electromechanical memories (10 ms). Studies indicate that the speed of computation would be greatly improved, and the memory cost reduced, if a memory existed which filled the gap. Such a memory must be intermediate between the electronic and electromechanical memories in cost and capacity as well as speed (Fig. 1).

It is proposed to use a memory based on electroplating for this purpose. Experiments described in Section III indicate that operation with the required characteristics may be feasible. However, some important problem areas are also uncovered and the proposed memory must therefore be viewed as speculative until solutions to these problems are found. It should be pointed out, however, that based on the state of current electrochemical theory no fundamental reason exists as to why the goals may not be achieved.

The advantage of an intermediate speed memory in increasing the speed of computation can be seen by considering a two-level hierarchy with access times \( T_f \) and \( T_s \) to the fast and slow memories, respectively. The hit ratio \( h \) is defined as the fraction of the requests for a memory word which finds the word already residing in the fast memory. The average access time \( T \) is

\[
T = T_f + (1 - h) T_s,
\]

where it has been assumed that the access time in case of a miss is \( T_s + T_f \). If the condition

\[
\frac{T_s}{T_f} \leq \frac{1}{1 - h}
\]

is met, \( T \) approaches the access time of the fast memory. Otherwise the slow memory dominates the access time.

The extent to which \( h \) can be made to approach 1 is determined by the capacity of the fast memory, the page size, the page replacement algorithm, and the program. The hit ratio between the main memory and the electromechanical memories may be in excess of 0.99, but hit ratios below 0.8 are also frequently encountered [2]. However, \( T_s/T_f = 1000 \) across the memory access gap, and (2) requires that \( h \geq 0.999 \), which is unreasonable on a sustained basis [2]. On the other hand, an intermediate memory with an access time in the range 100 to 1000 μs would allow the system to operate essentially at the speed of the main memory.

The desirable characteristics of the intermediate memory can be seen from Fig. 1. The access time must be 100 μs to 1 ms, and the capacity must be 10⁸ bits. The projected cost must take into account the expected decrease in the price of memories. A cost of 0.1 cents/bit is therefore projected. Since this figure is the system cost, a stack cost of 300 cents/bit is indicated. It is expected, however, that the proposed memory will actually be an order of magnitude cheaper than this target figure.

A memory which satisfies the above specifications must be as follows:

1) electronic (no moving parts);
TYPICAL SYSTEM COST PER BIT

<table>
<thead>
<tr>
<th></th>
<th>50¢</th>
<th>10¢</th>
<th>3¢</th>
<th>0.3¢</th>
<th>0.01¢</th>
</tr>
</thead>
</table>

TYPICAL ACCESS TIME

<table>
<thead>
<tr>
<th></th>
<th>50 ns</th>
<th>500 ns</th>
<th>5 µs</th>
<th>10 ms</th>
<th>40 ms</th>
</tr>
</thead>
</table>

TYPICAL CAPACITY (BITS)

<table>
<thead>
<tr>
<th></th>
<th>(10^5)</th>
<th>(10^6)</th>
<th>(10^7)</th>
<th>(10^8)</th>
<th>(10^9)</th>
</tr>
</thead>
</table>

Fig. 1. Memory hierarchy characteristics.

II. ELECTROLYTIC MEMORY

A binary cell of the proposed memory is shown in Fig. 2. Two electrodes are immersed in an electrolyte. In Fig. 2(a) both electrodes are inert and a limited amount of metal is available for electrodeposition. If this metal is on the left-hand electrode a 0 is stored. If the metal is on the right-hand electrode a 1 is stored. Fig. 2(b) shows a variation where the 0 electrode is fabricated of the electrodeposited metal. To store a 1 a small amount of this metal is transferred to the inert electrode.

To read, it is attempted to pass current in the 0 direction. If a 1 has been stored, metal deplates from the 1 electrode onto the 0 electrode and current flows. If a 0 has been stored, no plating can take place and no current flows. To write a 1 following a read, current is passed in the opposite direction to plate on the 1 electrode. To write a 0 no current is passed. This read/write method is analogous to core memories.

Fig. 3 shows a possible implementation of the memory plane. The \(N_x\) \(x\)-conductors and \(N_y\) \(y\)-conductors are photolithographically fabricated on suitable substrates.

2) mass-fabricated;
3) preferably noncirculating random access.

The last requirement can be seen as follows. If a 100-µs average access time is required and a circulating memory is used with a bit rate of 4 Mbits/s, read/write stations must be supplied at intervals of 800 bits. Such stations add materially to the cost of the memory. Further, the bits come out at least partially serially, thereby adding to the access time. By contrast, a random-access coincident-select organization reduces the amount of the read/write circuitry, and the parallel access to the bits provides a better match organizationally with the electronic memory (with which the large majority of the transactions takes place).
The arrays are immersed in the electrolyte a small distance $D$ apart. A bit is stored at each crossover for a total of $N_x N_y$ bits in the plane. Typical dimensions may be 0.001-in-wide conductors on 0.003-in centers. The array spacing $D$ is approximately the same as the conductor width, i.e., 0.001 in. It is important to note that the economics which force the bit size of semiconductor, bubble and disk memories to be of the order of micrometers are not operative here. Because of the extreme simplicity of the electrolytic storage array the array cost is negligible and the memory cost will be dominated by the cost of interconnection with the driving and sensing electronics. Thus the cell size and array dimensions will be determined primarily by convenience in fabrication and interconnection. With the dimensions given, the volume of the memory is still small. A $6 \times 6$ in array can store $4 \times 10^4$ bits, and if the substrates are 0.050-in-thick, 25 memory planes occupy a space of $6 \times 6 \times 2\frac{1}{2}$ in (exclusive of electronics) and store $10^6$ bits. It is seen that if dimensions larger than postulated are optimum from the standpoint of fabrication and interconnection, the memory is still reasonable in size.

Each proposed memory plane carries its own IC decoding, driving, and sensing electronics. The number of interconnections with the outside world is relatively small and consists of the address bus, data bus, and power supply leads. On the other hand, the number of interconnections between the IC chips and the selection conductors is large. The $6 \times 6$ in plane above requires $4 \times 10^8$ interconnections with the IC chips. The memory cost may be estimated as follows. Assuming a total of 20 MOS transistors per drive line and an IC cost of 0.1 cents per transistor, the IC cost is 2 cents per drive line. Assuming an interconnection cost of 3 cents per drive line, the total cost per drive line is 5 cents. This is prorated among $10^8$ bits for a stack cost of 5 cents/bit. (It is assumed that the cost of the conductor array and electrolyte is negligible by comparison.) The figure of 5 cents/bit is much smaller than the targeted 30 cents/bit and indicates that the cost of the proposed memory may overlap with that of the electromechanical memories.

Bit selection in the proposed memory is of a random-access coincident-voltage type. The $x$-conductor passing through a given bit is driven to a voltage $V_{1/2}$, and the $y$-conductor is driven to $-V_{1/2}$. The voltage $V_{1/2}$ is insufficient to cause current flow even if plating in the selected direction is possible. Only at the selected bit is there a full-select voltage $V_f = 2V_{1/2}$. This voltage is sufficient to cause current flow if plating in the selected direction is possible. If plating in the selected direction is not possible, no current will flow even with $V_f$ applied. Fig. 4 shows the voltage and current at a selected bit in a write/read cycle. A close analogy with core memories exists.

Successful operation of the proposed memory depends on the existence of a switching threshold, i.e., a voltage $V_{fr}$ below which no plating can occur. Then $V_{1/2} < V_{fr} < V_f$. Such thresholds are called overpotentials in electrochemistry. The voltage across an electrochemical cell carrying current is composed of the following parts:

1) The standard electrode potential, modified by corrections for the concentration ("activity") of the ions.

2) The activation overpotential, which is caused by the activation energy of getting the ions onto or away from the electrodes. This is analogous to the work function of a cathode.

3) The concentration overpotential: this is a further correction to the standard electrode potential caused by the fact that with current flowing the concentrations of the various species on the electrode or in the vicinity of the electrode can depart radically from the equilibrium concentration.

4) Overpotential due to passivation: many metals will form protective oxide or other layers under certain conditions of pH and applied potential. Then the applied potential must be changed sufficiently to redissolve the protective layer before deplating can occur.

5) Ohmic drop in the electrolyte: in plating metal from one electrode to the other the standard electrode potentials cancel since the process at one electrode is just the negative of the other. (It is important to note also that the proposed electrolytic memory cell will not exhibit a "battery potential" because no porous membrane segregates the ions. Thermodynamic equilibrium is reached at 0 $V$ poten-
The concentration overpotential will not be significant because the short bipolar current pulses will not appreciably disturb the equilibrium concentrations of the various ionic species. Ohmic drop is undesirable and will be minimized by cell geometry and electrolyte chemistry. Thus the threshold $V_{th}$ must be obtained by a suitable choice of electrolyte and electrode so as to either obtain an adequate activation overpotential or to passivate the electrode.

Ideally, no current should flow for any applied voltage when no plating is possible, such as in reading a 0. However, competing chemical reactions are always waiting in the wings and current will flow when some threshold $V_{th}$ is exceeded. $V_{th}$ in the sum of the standard electrode potentials for the undesired reaction and the appropriate overpotentials. An important design parameter in the proposed memory is $V_a > V_f$ to ensure that the full-select voltage does not initiate the competing chemical reaction.

A problem with the simple system of Fig. 3 is that the full-select voltage $V_f$ exists between the entire length of the selected $x$-conductor and the selected $y$-conductor. Although the electric field lines in the electrolyte are concentrated in the vicinity of the selected bit, a small amount of undesired plating may take place elsewhere. It may therefore be necessary to construct the plane so that an isolated volume of electrolyte is associated with each intersection. Although it does not seem worthwhile to draw up detailed construction schemes until the magnitude and nature of the problem are fully appreciated with respect to the particular electrode–electrolyte system used, a possible construction is shown in Fig. 5. The $x$-conductor plane is first bonded to the spacer. The resulting microcontainers are then filled with the electrolyte and the $y$-conductor plane is bonded on top. This construction has additional advantages as well. The capacitance of the conductors is reduced by reducing the area of contact with the electrolyte. Also, the electrolyte is hermetically sealed against contamination from the atmosphere—such sealing will probably be necessary in any case. A third and less obvious advantage is that the small volume of electrolyte limits the number of impurity ions which can come in contact with the electrode. By contrast, in the scheme of Fig. 3 new impurity ions can be brought in by convection. This aspect of the problem will be discussed later.

The idea of using electrodeposition as a basis for memory is not completely new. Several patents [3]–[6] on electrochemical memories have been issued. All of these except [6] differ considerably in geometry and purpose of application from the memory proposed here. Reference [6] proposes coincident-voltage selection, but the method of cell operation differs significantly from the one proposed here. The writer is not aware of any publication other than the patents in this area.

III. EXPERIMENTAL RESULTS

A. $I$–$V$ Characteristics

The experiments were aimed primarily at determining whether electrodeposition on the required time scale (100 ms to 1 ms) is possible, to investigate the threshold characteristics and read discrimination, and to identify problem areas. Gold electrodes were used and copper was plated in a CuSO$_4$ electrolyte. The $I$–$V$ characteristic of this system with 1 M CuSO$_4$ is shown in Fig. 6. The data are taken as follows. Starting with a plated electrode and a clean electrode a voltage is applied with the plated electrode negative (third quadrant of Fig. 6). No addi-
tional electrodeposition can occur and the current is zero until a threshold of 1.5 V is exceeded. Above this threshold additional copper is plated on the cathode and gas is liberated at the anode. The reaction is

$$\text{Cu}^{+} + \text{H}_2\text{O} \rightarrow 2\text{H}^+ + \text{Cu}^{\text{(plated)}} + \frac{1}{2}\text{O}_2\text{(gas)}.$$  \hspace{1cm} (3)

This represents an unwanted chemical reaction with $V_{t1} = 1.5$ V. The threshold is the sum of the standard electrode potential for this reaction (0.89 V), a correction for the $p\text{H}$, i.e., the $\text{H}^+$ ion concentration (−0.18 V), and the overpotential ($\approx$0.8 V). Since the overpotential due to the Cu deposition is small this overpotential is primarily due to the oxygen evolution (oxygen overpotential). Ohmic drop along with the voltage dependence of the overpotential is responsible for the additional voltage at higher currents.

The applied voltage is now reversed so that the plated electrode becomes positive. Current flows almost immediately (first quadrant of Fig. 6). This branch of the curve must be plotted while electrodeposition is in progress. When all the available copper has been transferred to the cathode the current drops to zero. The $I$−$V$ characteristic has now shifted along the abscissa so that $V_{t2}$ appears on the right.

Experiments with various electrolyte concentrations and electrode geometries indicate that the voltage drop in the “forward” direction is almost entirely ohmic. The overpotential due to copper deposition is in the range of millivolts. Thus this electrode–electrolyte system exhibits a very low threshold $V_{t1}$ and is therefore not suitable for the proposed memory. Nevertheless, experiments on dynamic behavior have been carried out on this system.

Fig. 5. Exploded view of a 4-bit section of a memory plane with isolated electrolyte pockets.

Fig. 6. $I$−$V$ characteristic of 1M CuSO$_4$ solution with gold electrodes.
because it was felt that the results would be representative of the dynamic behavior of cells in general.

B. Capacitance and Conductance

Fig. 7(a) shows a simple equivalent circuit of the cell when it is operating in a region of 0 dc current. R is the ohmic resistance of the electrolyte and is a function of the electrode geometry and spacing. C₁ and C₂ are the capacitances between the electrodes and the electrolyte. These are independent of the electrode spacing and are simply proportional to the electrode areas. The read discrimination (1/0 ratio) is determined by the electrode capacitance and therefore an understanding of this capacitance is important.

The experimental cell for capacitance measurement consists of two clean gold electrodes (no copper) in CuSO₄ electrolyte. The applied voltage is always kept below Vₐ. The step response of this cell is shown in Fig. 7(b). Two different processes are occurring. The current is initially exponential and is determined by the RC time constant of the cell and the external circuitry. The capacitance in this region is due to the charging of the double layers at the two electrodes. The double layer is a charge layer which appears at an electrode-electrolyte interface and is analogous to the depletion layer in semiconductors, although it differs considerably in structure [7]. The charging of the double layer follows the rise of the voltage across C₁ and C₂ without delay on the time scale of interest (microseconds). However, the charging current does not diminish to 0 exponentially but exhibits a long tail as shown in Fig. 7(b). This tail, which can last as long as 100 ms, is believed to be due to chemical reactions involving trace impurities in the electrolyte. Its length is determined by the rate of the chemical reaction and not simply by the circuit time constant. However, the circuit influences the rate of the chemical reaction as will be discussed later. As a specific illustration of the kind of reaction which may be involved, assume the presence of a small concentration of ferrous ions in the solution. Then a small amount of copper can be plated by the reaction

\[ 2\text{Fe}^{++} + \text{Cu}^{++} \rightarrow 2\text{Fe}^{+++} + \text{Cu}. \] (4)

The equilibrium of this reaction is shifted slightly to the right when the electrode is pulsed negative, and thus even unipolar pulses can cause a small amount of plating and deplating on the electrode. A similar effect can be obtained from cuprous ions and other impurities. It is important to stress that truly minuscule amounts are involved, typically \(10^{12}\) atoms/cm². By comparison a smooth monolayer of plating would contain approximately \(10^{16}\) atoms/cm².

A major experimental difference between the two processes is reproducibility. The initial capacitance, due to the double layers, does not depend on trace impurities and is extremely reproducible. The charge accumulated in the tail, on the other hand, can be reduced by a large factor by the following process: a third electrode at a negative potential \(|V| < |V_a|\) is immersed in the electrolyte for several seconds and then removed. In this manner some Cu is removed from the solution and the impurities are left in a more oxidized state thereby decreasing the magni-
tude of the reaction (4). A second difference between the two processes is that the double layer capacitance varies relatively slowly with the applied voltage $V_{\text{step}}$, while the charge accumulated in the tail is a strong function of $V_{\text{step}}$.

The following experimental data were taken with the electrolyte oxidized by the technique just described. It should be remembered that the measured capacitance $C$ is a series combination of $C_1$ and $C_2$. No effort has been made to distinguish the individual electrode capacitances. These are generally unequal since one electrode is moving positive with respect to the electrolyte while the other is moving negative.

Fig. 8 is a plot of the capacitance per unit area $C(t)$ as a function of time ($V_{\text{step}}$ is applied at $t = 0$). The electrolyte is at 1M concentration. $C(t)$ is defined as $C(t) = Q(t)/V(t)$ where $Q(t)$ is the integrated current density and $V(t) = V_{\text{step}} - I(R_{\text{source}} + R)$ is the instantaneous voltage across the capacitors. In this setup the time constant of $V(t)$ is of the order of 100 $\mu$s. The two capacitance mechanisms are clearly observable in Fig. 8. The constant capacitance for times less than approximately 100 $\mu$s is due to the double layer capacitance and varies relatively slowly with $V_{\text{step}}$. After 100 $\mu$s, additional charge accumulation attributed to reactions with impurities is observed. The rate and amount of accumulated charge varies rapidly with $V_{\text{step}}$. The approximate linearity of the curves in Fig. 8 suggests that $I(t) \approx 1/t$ in the tail region, at least for the 0.2 V and 0.5 V cases. Obviously, $I(t)$ must decrease faster than $1/t$ for large $t$, otherwise infinite charge would accumulate.

In interpreting Fig. 8 it must be kept in mind that because the rate of charge accumulation due to the impurities is a strong function of the instantaneous voltage $V(t)$, rapid charge accumulation begins only when $V(t)$ reaches a large fraction of its steady-state value $V_{\text{step}}$. Hence the time duration of the constant-capacitance region is related more to the rise time of $V(t)$ than to intrinsic factors. Fig. 8 shows that the charging of the electrode-electrolyte interface is a complex process which cannot be accurately described by a single number (capacitance). This means, unfortunately, that the dependence of the read discrimination on pulse amplitude, duration, and rise time must be determined largely empirically.

The conductance and capacitance of the cell are functions of the electrolyte composition and the condition of the electrodes. Since in the proposed memory the signal is an ohmic (plating) current and the noise is a capacitive current, it is advantageous to maximize the conductance/capacitance ratio of the cell. Fig. 9 shows experimental curves for the capacitance and resistivity of this system as a function of the CuSO$_4$ concentration, at $V_{\text{step}} = 0.5$ V. Two capacitance curves are shown corresponding to two different times in Fig. 8. $C(t = 0)$ measures the double layer capacitance and $C(t = 20$ ms) is a measure of the additional charge accumulation in the tail. The slight discrepancy in $C(t = 20$ ms) between Figs. 8 and 9 illustrates the reproducibility problem previously discussed. The resistivity was calculated from the current amplitude at $t = 0$ (see Fig. 7). It is to be remembered that no dc current flows in this experiment. The conclusion drawn from this graph is that the solution should be as concentrated as possible. The capacitance increases very slowly with increased concentration, whereas the resistivity decreases very rapidly.

In electroplating practice H$_2$SO$_4$ is always added to the CuSO$_4$ bath. This increases the conductance of the bath and speeds up the electrodeposition. The mechanism which achieves this is less obvious than might at first appear, since the H$^+$ and SO$_4^{2-}$ ions do not react at the electrodes and therefore do not carry current. Under dc conditions the effect of the additional ions ("indifferent electrolyte") is to redistribute the potential drops in the cell so that more of the applied voltage is available to overcome the overpotentials [8]. It can be shown that this results in an increased electrodeposition rate [9]. (However, the relevance of the dc theory to the transient conditions of present concern is not clear a priori.)

Fig. 10 shows experimental curves for the capacitance and resistivity of the CuSO$_4$-H$_2$SO$_4$ system as a function of pH. The sulfuric acid was added to 1M CuSO$_4$ and the step voltage was 0.5 V. It is seen that the capacitance is relatively insensitive to pH, while the resistivity decreases.
rapidly with acidity; this suggests that adding an indifferent electrolyte may be a route to increased signal-to-noise ratio. Adding $H_2SO_4$ does not affect the $I-V$ characteristics of Fig. 6 except for the decreased ohmic drop.

The fact that the double layer capacitance is relatively insensitive to electrolyte composition and concentration (for all but the most dilute electrolytes) has been explained theoretically [7]. The relevance of this fact to the present work is that one can maximize the read discrimination of the memory by simply choosing the electrolyte which yields the maximum electrodeposition rate.

One of the most important factors bearing on the cell characteristics is the cleanliness of the electrodes. Extremely thin films of organic material, purposely applied or inadvertent, dramatically affect the cell characteristics. In the experiments discussed so far the electrodes have been meticulously cleaned. The general effect of an organic film is, however, beneficial. The capacitance decreases dramatically without a corresponding decrease in the cell conductance or the transient electrodeposition rate. This effect is tentatively understood as follows. The presence of an organic film decreases the area of the electrode in contact with the electrolyte, thus proportionally decreasing the capacitance. This is supported by microscopic examination of thick electrodeposits: the copper grows on isolated islands covering a small fraction of the surface. The rate of electrodeposition is, however, not correspondingly affected since the bulk of the solution is still available for ion transport (Fig. 11). In other words, thicker deposits grow in smaller areas.

Fig. 12 shows the capacitance of gold electrodes coated with a thin film of petroleum jelly. The electrolyte is pure 1M $CuSO_4$ and $V_{step} = 0.5$ V. Comparison with Fig. 9 shows that $C$ has decreased by a factor of 10. The capacitance depends entirely on the degree of coverage and can be changed at will. Coating the electrodes has, of course,
no effect on the electrolyte resistivity. The effect on the electrodeposition rate will be discussed in the next section.

C. High-Speed Operation

In order to optimize the read discrimination of the memory it is necessary to maximize the cell conductance/capacitance ratio. The capacitance may be reduced by coating the electrodes as just discussed. The conductance may be increased by using a concentrated electrolyte and/or by adding an indifferent electrolyte. A third, and most important, way to increase the conductance is to use small electrode spacing. Fortunately, this requirement is consistent with the requirement due to fabrication technology (Fig. 5), and is also desirable in order to minimize the impurity reactions such as (4). A small volume of electrolyte contains fewer impurity atoms and it is experimentally verified that the electrodeposition is more stable, i.e., oxidizes slower, when the electrolyte volume is small.

Although the experiments described in the previous section point the way to improved memory cell performance, many of the conditions are different in the actual memory cell. First, there is some electrodeposited copper on at least one of the electrodes. Second, the conductance is determined partly by the dynamics of the electrodeposition rather than only by the bulk resistivity of the electrolyte. Although the discussion in connection with Fig. 6 indicates that the overpotential connected with the electrodeposition is small, that conclusion applies only to a dc situation. In a dc situation copper is plating on copper, whereas in the transient the plating is on the gold surface. Thus there are many unknowns which can be resolved only by operating the cell in the memory mode.

The experimental memory cell consists of two 0.021-in diameter gold wires encased in Teflon plungers so that only their flat ends are exposed to the electrolyte. The electrode spacing can be varied by a micrometer adjustment.

Fig. 13 shows the step response of the cell as a function of electrode spacing. \( V_{\text{step}} = 0.5 \) V and the electrodes are clean and have no deposited copper. The electrolyte is 1M \( \text{CuSO}_4 \) and has been oxidized as previously described. The two regions in Fig. 7(b) are clearly distinguished in the current waveform for 0.001-in spacing. Because the electrode area is much smaller than in the previous experiments, \( V(t) \) rises faster and the time scale is compressed compared to Fig. 8. The photographs clearly indicate that the capacitance is independent of the electrode spacing and that the double layer charging transient is faster at smaller spacing.

A dramatic change in the accumulated charge (hereafter referred to as the noise pulse) occurs when copper is deposited on one of the electrodes (Fig. 14). The 0.5-V voltage pulse is 0.5 ms long and both the rising and falling transients are shown. Unipolar pulses are applied with the plated electrode negative so that no electrodeposition occurs. The noise pulse is approximately two orders of magnitude larger in area than in Fig. 13 (see Table 1). The additional charge is interpreted on the basis of (4). Some of the deposited copper is oxidized and goes into the solution leaving many impurity atoms in the electrolyte in a reduced state. This greatly increases the magnitude of reaction (4). The disappearance of copper from the electrode is easily verified experimentally by plating back and forth and observing the reduction in the plating
Further, the addition of an oxidizing agent such as potassium dichromate reduces the noise pulse (unfortunately it also oxidizes the copper on the electrode). It should be noted that even in Fig. 14 the amount of copper transferred is minute: approximately $3 \times 10^{12}$ atoms which is equivalent to one monolayer. The large noise pulse in the presence of copper places a major limitation on the signal-to-noise ratio of this memory cell and a requirement of the chemical system used will be the absence of such an effect.

Fig. 15 shows the memory operation of this cell. Fig. 15(a) shows the pulse program, which is a WRRWRR⋯ sequence of 0.5-V 5-ms pulses. Fig. 15(b) shows the current in the cell. Electrodeposition (switching) current flows under the WRITE pulse from the 0 to the 1 electrode and returns under the first READ pulse to the 0 electrode. The current under the second READ pulse is the noise pulse. In Fig. 15(c) the pulses under the two READ pulses are superimposed to better indicate the READ discrimination. The READ discrimination is better when the electrode spacing is smaller, as expected. It is seen that good discrimination is not possible for pulses shorter than approximately 2 ms in this system. The amount of copper plated at an electrode spacing of 0.001 in in Fig. 15 corresponds to approximately six monolayers, although it is unlikely that the copper actually deposits uniformly.

Much better operation is observed in an electrolyte consisting of 1M CuSO₄ acidified to pH = 0.0. The noise pulse is essentially the same as in pure CuSO₄, both with and without copper on the electrode. The amount
TABLE I
**Summary of Switching Characteristics**
(Approximate Area Under Pulse)  
(Electrode Area: 346 mils²  Electrode Spacing: 1 mil)

<table>
<thead>
<tr>
<th>Electrolyte</th>
<th>Electrode Condition</th>
<th>Excitation</th>
<th>Noise Pulse (nC)</th>
<th>Signal (Switching) Pulse (nC)</th>
<th>Fig.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1M CuSO₄</td>
<td>uncoated unplated</td>
<td>0.5 V, 0.5 ms unipolar</td>
<td>10</td>
<td>—</td>
<td>13</td>
</tr>
<tr>
<td></td>
<td>uncoated plated</td>
<td>0.5 V, 0.5 ms unipolar (plated electrode negative)</td>
<td>1000</td>
<td>—</td>
<td>14</td>
</tr>
<tr>
<td></td>
<td>uncoated plated</td>
<td>WRITE: 0.5 V, 5.0 ms</td>
<td>1000</td>
<td>8000</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>READ: 0.5 V, 5.0 ms</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1M CuSO₄ + H₂SO₄</td>
<td>uncoated unplated</td>
<td>0.5 V, 0.5 ms unipolar</td>
<td>10</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>uncoated plated</td>
<td>0.5 V, 0.5 ms unipolar (plated electrode negative)</td>
<td>1000</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>uncoated plated</td>
<td>WRITE: 0.5 V, 5.0 ms</td>
<td>1000</td>
<td>20 000</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td>READ: 0.5 V, 5.0 ms</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>uncoated plated</td>
<td>WRITE: 0.8 V, 500 µs</td>
<td>2000</td>
<td>5000</td>
<td>16</td>
</tr>
<tr>
<td></td>
<td></td>
<td>READ: 1.0 V, 500 µs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1M CuSO₄</td>
<td>coated unplated</td>
<td>0.5 V, 0.5 ms unipolar</td>
<td>10</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>with or without</td>
<td>coated plated</td>
<td>0.5 V, 0.5 ms unipolar (plated electrode negative)</td>
<td>100</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>H₂SO₄</td>
<td>coated plated</td>
<td>0.5 V, 0.5 ms unipolar (plated electrode negative)</td>
<td>150</td>
<td>400</td>
<td>17</td>
</tr>
<tr>
<td>1M CuSO₄ + H₂SO₄</td>
<td>coated plated</td>
<td>WRITE: 1.2 V, 50 µs</td>
<td>150</td>
<td>400</td>
<td>17</td>
</tr>
<tr>
<td></td>
<td></td>
<td>READ: 1.0 V, 100 µs</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Fig. 15. Memory operation: uncoated electrodes, 1M CuSO₄. (a) Pulse program. (b) and (c) Cell current.
of copper transferred in switching, however, increases by approximately a factor of 2.5 under identical conditions (see Table I). Fig. 16 shows the read discrimination with 500-μs pulses. The pulse program is the same as in Fig. 15 and the pulse amplitudes are $V_{\text{write}} = 0.8 \text{ V}$, $V_{\text{read}} = 1.0 \text{ V}$. These voltages are below $V_{\text{r2}}$.

Further improvement can be obtained by coating the electrodes to decrease the capacitance. It is found that the noise pulse in the presence of copper on the electrode decreases by the same ratio as the noise pulse without copper, typically a factor of 10 (see Table I). The copper transferred during switching decreases by approximately a factor of 2, indicating that the rate of copper deposition is hindered somewhat by the smaller available area. A considerable improvement in read discrimination is obtained, allowing even faster operation. Fig. 17 shows the read discrimination in an acidified electrolyte ($pH = 0.0$) under the following pulse conditions: $V_{\text{write}} = 1.2 \text{ V}$, 50 μs; $V_{\text{read}} = 1.0 \text{ V}$, 100 μs. The read pulse is made longer to ensure that all the copper is returned during read. This figure demonstrates good discrimination at a speed which easily meets the goal of the proposed memory. At 0.001-in electrode spacing the amount of copper plated would amount to approximately 0.25 mono-layers if it were uniformly distributed over the entire (uncoated) electrode area.

When copper is first introduced onto the electrode it tends to quickly oxidize and disappear from the electrode. A stable copper deposit can be obtained by adding copper until a sufficient number of impurity ions has been reduced to bring the reaction into balance. The penalty paid for this is the large noise pulse obtained (Fig. 14). A stable deposit so obtained tends to oxidize further over a time scale of minutes to hours, presumably due to atmospheric contamination of the electrolyte.

There is no deterioration in the read discrimination as the repetition rate is increased to the maximum compatible with the pulse durations used. On the other hand,
if the delay time between the write pulse and the subsequent read pulse is increased a decrease in the "read 1" signal takes place up to a delay time of 100 ms. This is attributed to the oxidation of the copper deposit which takes place far into the tail of the waveform of Fig. 14. The read discrimination stabilizes after approximately 100 ms, and useful signals have been obtained for delay times of several minutes. For very long times the further oxidation of the copper due to atmospheric contamination degrades the performance.

Since the dc characteristic of Fig. 6 may not give a true picture of the threshold $V_n$ under dynamic operating conditions the disturb sensitivity was investigated in the memory mode. The results confirmed that very little selection threshold exists in this system.

IV. CONCLUSIONS

Fig. 17 illustrates that good read discrimination can be obtained on the time scale of interest in the proposed memory. It is obvious, however, that the read discrimination is not sufficiently good to operate the bit in a large array where the noise of all the half-select bits adds up. The situation would be quite different if the noise pulse with copper (Fig. 14) were the same as the noise pulse without copper (Fig. 13). Then the noise pulse in Fig. 17 would be one hundred times smaller in area and the read discrimination would be better than in magnetic cores. Assuming that such a situation is attainable, a simple read discrimination calculation pertaining to a $4 \times 10^6$ bit memory plane is made below.

A capacitance of 0.3 $\mu$F/cm² is assumed (Fig. 12). The $t = 0$ capacitance is the valid figure to use in calculating the peak noise current, since the charge accumulation due to impurities is assumed absent. The capacitance of a 1 mil² bit is $C_{bit} = 1.9$ pF. Assuming a half-select voltage $V_{1/2} = 0.5$ V and a voltage pulse rise time $T_{rise} = 10$ $\mu$s, the peak half-select current is $I_{noise}$ (bit) = $2C_{bit} V_{1/2} T_{rise} = 0.19$ $\mu$A. The peak occurs approximately 5 $\mu$s after the initiation of the pulse. For a selection conductor $2 \times 10^9$ bits long the noise current is $I_{noise}$ (line) = 380 $\mu$A. The signal (plating) current in 1 bit is, by using Fig. 17 and scaling down the bit size, $I_{signal} = 29$ $\mu$A. Fig. 18 shows the read discrimination of the memory plane. The read discrimination compares well with core planes and the sensing techniques used there, such as strobing and common-mode rejection, are applicable here.

A further note of interest is the small voltage ($\approx 1$ V) and current ($\approx 1$ mA) needed to drive the selection lines. Such voltages and currents are easily obtained from small-area integrated circuits without the need for special driver circuits. This is a very important consideration since the peripheral circuitry is an important component of the memory cost.

Although the experimental results are encouraging, three important problem areas have been identified. These are to obtain an adequate selection threshold $V_n$, to reduce the effective electrode area, and to greatly reduce or eliminate the reaction of the deposited metal with impurities. This last requirement is necessary both to reduce the noise current and to ensure the long-term stability of the deposited metal. Approaches to solutions of these problems will now be summarized.

In order to obtain an adequate threshold $V_n$ it is necessary to use a system which exhibits a considerable overpotential on electrodeposition. Two possibilities appear to exist: first, to choose the electrolyte, electrodeposited metal, and electrode in such a way that a large activation overpotential exists on electrodeposition. For example, nickel is known to exhibit a large overpotential. Second, to choose an electrodeposited metal which passivates.

The effective electrode area can be reduced with a partial electrode coating. This coating does not have to be organic but it must be reproducible, amenable to large-scale manufacture, and must be absolutely stable.

The solution of the impurity problem will probably be the most difficult. The incredibly minute amounts involved have been pointed out. Since experiments so far have been in only one chemical system, it is difficult to forecast the magnitude of the problem in another system. It is possible for example, that the same mechanism which will be used to obtain a selection threshold will also inhibit the reaction of the deposited metal with the impurities. Hence the two problems may have a common solution. It will probably be necessary to hermetically seal the cell against atmos-
pheric contamination, to use a small volume of electrolyte, and to purge the electrolyte of those ions which can oxidize the deposited metal or reduce the metal ions.

The electrochemical problems to be solved open up the fascinating and almost completely unexplored area of high-speed transient electrochemistry. Much that is known about de electrochemistry is not relevant here. For example, in electropolating “practice” a current density of 0.1 A/cm² is considered high; in the transient of Fig. 17 the current density is 5 A/cm² prorated over the entire electrode area; it is much greater in the vicinity of the electrodeposited islands. The reason why this is possible is that the ion concentrations near the electrodes do not appreciably change during the transient. Even when a given bit is repeatedly addressed, the current alternates in direction and the ion concentrations remain at their equilibrium values.

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REFERENCES


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A Geometric Model for Stochastic Automata

FRANCOIS BANCILHON

Abstract—This paper is concerned with the problem of equivalence and dominance relations between sequential stochastic machines. We first introduce the transition output stochastic automaton together with the notion of pseudoautomaton. In Section III, we establish some fundamental properties concerning the rank of a stochastic automaton.

This yields the definition of a geometrical stochastic automaton (GSA), using the notion of polyhedral cones introduced in Section II. Section V is a systematic investigation of the set of GSA's, mainly concerned with the relations between two GSA's.

In Section VI we establish relations between a GSA and a stochastic automaton. Section VII proves the interest of the geometrical model by applying properties of GSA's to stochastic automata, to solve an open problem concerning minimization.

Index Terms—Cones, dominance, equivalence, geometric model, stochastic automata.

I. THE TRANSITION-OUTPUT STOCHASTIC AUTOMATON

Definition 1: A transition-output stochastic automaton, as introduced by Carlyle [1], is defined through the specification of three finite sets:

\[ X = \{x_1, x_2, \ldots, x_n\} \text{ is the input alphabet,} \]

\[ Y = \{y_1, y_2, \ldots, y_m\} \text{ is the output alphabet} \]

\[ R = \{r_1, r_2, \ldots, r_p\} \text{ is the set of pure states} \]