an array using a state-partitioning technique. The array is easy to form; it can be formed by hand even for quite large machines. Inspection of the array indicates whether or not UD's or SR's can be used to mechanize the machine, and if they can, the necessary state assignment is easily obtained from the array.

Finally, it is noted that SR and UD realizations often require fewer interconnections between units than do standard flip-flop realizations; this may make them attractive in certain MSI and LSI systems.

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Multifunction Threshold Gates

DANIEL HAMPEL

Abstract—Threshold logic gates, up to now, generally have been presumed to provide a single function of the input variables. The threshold gates that have been integrated [1]–[4] were naturally double-sided and provided complementary outputs or, more specifically, complemented dual outputs. This paper shows that the in-phase and out-of-phase outputs can, in fact, be designed to provide grossly different functions of the input variables. Two examples of this technique have already been shown [5] and one of these, the full adder, has been demonstrated in a multiplier [6]. Now this technique is generalized, and furthermore, it is shown how each side can be subdivided to provide a number of functions simultaneously. Finally, virtual ORing of specific output points from each side will result in still more functions. The sum-resistor specification for any order function on either side is given. Practical application of these techniques are discussed, including those basic ones that have already been disclosed.

Conventional threshold logic has already been shown to provide improvements compared to NAND or OR/NOR gates in such factors as versatility, interconnection complexity, component count, power, and speed. The multifunction threshold-gate approach will further improve these factors for many applications.

Index Terms—Emitter coupled logic, high-speed logic, multifunction logic, parity circuits implemented with threshold logic, threshold logic, universal logic, virtual ORing.

Introduction

This paper shows how current-summing threshold gates can be used to provide two or more threshold functions simultaneously. First, a brief background is given on the threshold gates that have been built at RCA for the past five years. Then, relationships are derived for summing resistors to produce different threshold functions of the inputs. It is shown how these summing resistors can be subdivided into a series of smaller resistors, the output of each giving still more threshold functions. Finally, virtual (or wired) OR connections between various combinations of the resis-

References


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tor network are used to obtain more functions. Some limitations and applications of these circuits are shown, and comparisons are made between the multifunction threshold-logic approach and the conventional threshold logic for these applications.

**BACKGROUND**

Integrated threshold gates have been designed and fabricated [1]–[6] using the following elements.

1) Current switches—for comparing each binary input to a reference and providing weighted currents.
2) Summing resistors—for summing the currents of all the switches in a gate.
3) Emitter followers—to reestablish the levels of the summing resistor and drive other gates.

An n-input threshold-gate schematic is shown in Fig. 1(a) with its logic symbol. The in-phase output (OUT) would be high when n or more inputs are high, while the out-of-phase output (OUT) would be low when n or more inputs are high.

Each gate naturally provides two outputs, as do ECL gates: an output in its true or in-phase side, and its complemented dual on the other side. Without constant-current sources for the differential current switches, the summing resistor on the inverted side is somewhat less than its nominal value to account for a higher current on that side when an input is higher than the reference; these sum resistors can be made identical if constant-current sources are used, and tolerances can be improved. The sum resistor on the in-phase side can be specified so that, for an n-input gate, the output is high (a binary 1) when m or more inputs are high, otherwise it is low. This resistor is the threshold control; circuits have, in fact, been integrated with threshold or m equal to n/2 (a majority gate) as well as m equal to n (an AND gate). In each case, the inverting outputs would provide the majority and NOR functions, respectively.

Fig. 1(b) shows symbols for the building-block elements based on the use of constant-current switches, and Fig. 1(c) shows a new symbolic schematic for the gate; \( R_I \) and \( R_0 \) are selected to provide outputs above or below the reference voltage \( V_{\text{ref}} \), depending on whether a given number of high inputs out of \( n \) are present.

This paper shows how to use gates with different sum resistors to provide two different functions (other than complemented duals of each other) simultaneously. Further, by breaking a sum resistor on any side of the gate into a series of smaller resistors, a number of lower order functions are immediately realized on either side. Both techniques result in a large savings in component count, power, and connections as compared to the use of regular threshold logic, where a gate is normally restricted to provide a single function and its complemented dual.

Specific applications of this principle have already been shown [5] as a refinement of the threshold gate for improved logic power. In those applications, different summing resistors were used to obtain different functions at the two summing nodes of a cluster of input differential switches. One of those applications, the full adder, was successfully demonstrated in a multiplier [6]. The idea is now generalized to include sum-resistor subdivisions, and other applications are shown.

**SUM-RESISTOR SPECIFICATION FOR DIFFERENT THRESHOLDS**

In this section, the expressions for the in-phase \( R_I \) and out-of-phase \( R_0 \) summing resistors are derived as a function of the threshold desired \( T \), a unit-current determining resistor \( R_a \), and the fan-in of the gate. Fig. 1(a) shows a generalized n-input gate; the symbols used are defined as follows.

\[
\begin{align*}
n & \text{ Number of inputs to a gate (an input with a weight of two counts as two inputs).} \\
m & \text{ Number of inputs that are high.} \\
(n-m) & \text{ Number of inputs that are low.} \\
T_I & \text{ Desired threshold of the in-phase output; } \text{OUTPUT} = 1 \text{ if } m \geq T_I. \\
T_0 & \text{ Desired threshold of the out-of-phase output; } \text{OUTPUT} = 1 \text{ if } (n-m) \geq T_0. \\
R_I & \text{ In-phase sum resistor.} \\
R_0 & \text{ Out-of-phase sum resistor.} \\
V_{\text{ref}}_1 & \text{ Reference voltage to which all inputs are compared.}
\end{align*}
\]

The expression for \( R_I \) is determined first. There is a
unit of current $I_u$ in $R_I$ for every low input. Therefore, the output $\text{out}$ is low when

$$| (n - m)I_uR_I | > | V_{\text{ref}} |.$$ 

The output $\text{out}$ is high when

$$| (n - m)I_uR_I | < | V_{\text{ref}} |.$$ 

If $m$ is equal to $T_I$, the output is equal to $V_{\text{ref}}$ when

$$n - (T_I - 1/2) | I_uR_I | = V_{\text{ref}}.$$ 

By using $(T_I - 1/2)$ rather than $T_I$ for the number of high inputs required to reach the reference, the signal swing about the reference is maximized because the inputs are restricted to binary values. Therefore,

$$R_I = \frac{V_{\text{ref}}}{I_u} \frac{1}{n - (T_I - 1/2)}.$$ 

The fraction $V_{\text{ref}}/I_u$ can be represented by $R_u$, an equivalent unit resistance that ultimately depends on the choice of power supply and the constant-current bias $V_{\text{ref}}$ as well as on $V_{\text{ref}}$. The expression for $R_I$ is then given by

$$R_I = R_u \frac{1}{n - (T_I - 1/2)}.$$ 

In the case of $R_0$, there is a unit of current $I_u$ in $R_0$ for every high input. Therefore, the output $\overline{\text{out}}$ is low when

$$| mI_uR_0 | > | V_{\text{ref}} |.$$ 

The output $\overline{\text{out}}$ is high when

$$| mI_uR_0 | < | V_{\text{ref}} |.$$ 

If $m = T_0$, the $\overline{\text{out}}$ is equal to $V_{\text{ref}}$ when

$$(T_0 - 1/2)I_uR_0 = V_{\text{ref}}.$$ 

The expression for $R_0$ is then given by

$$R_0 = \frac{R_u}{T_0 - 1/2}.$$ 

Another way of interpreting the concept is to plot the sum point voltage at $R_0$ as a function of the number of high inputs ($m$) or the sum point voltage at $R_I$ as a function of the number of low inputs ($n - m$), as shown in Fig. 2. The output voltage, which is equal to the sum point level less the $V_{\text{ref}}$ drop of the emitter followers, crosses the reference at 1/2 for $T_0 = 1$ and $T_I = n$, 3/2 for $T_0 = 2$ and $T_I = n - 1$, and so on. The slopes of the characteristics represent the summing resistors, and the steepest slope corresponds to the NOR and AND functions.

**Series Resistors**

Given any $R_I$ or $R_0$, a series of resistors $R_{I1}, R_{I2}, \ldots$ or $R_{01}, R_{02}, \ldots$ can be used to furnish a number of lower order functions of each side simultaneously. The general case is shown in Fig. 3(a).

\[ R_{I1} = \frac{R_u}{n - (1 - 1/2)} \]

\[ R_{I2} = \frac{R_u}{n - (2 - 1/2)} - R_{I1} \]
The expression for each incremental value of resistor that gives the next higher order function is as follows:

\[
\Delta R_f = \left[ \frac{1}{n - (T_i + 1 - 1/2)} \right] R_a
\]
\[
\Delta R_i = \left[ \frac{1}{n^2 - 2nT_i + T_i^2 - 1/4} \right] R_a.
\]

Fig. 4 shows curves of these expressions, indicating the incremental values of series resistors needed to provide successive functions.

**Virtual ORing (Wired OR)**

If an \( n \)-input gate had all possible series resistors on both output sides, it would provide \( 2n \) functions of the \( n \)-input variables. Because each output would be derived from an emitter–follower connected to each resistor, virtual ORing can be achieved between certain pairs (one from the \( I \) side and one from the \( 0 \) side) of the \( 2n \) outputs to derive yet other functions [5]. For example, the NOR \( R_a \) can be ORed with the AND \( R_b \) to provide the matching function of the \( n \) inputs—all 1 or all 0. These connections are shown in Fig. 3(b).

The NOR output can also be ORed with each increasing \( I \) function (except the \( I_1 \) or OR function\(^1\)) to provide \( (n - 1) \) new functions. Similarly, the \( R_b(n-1) \) output can be ORed with each \( I \) function up to \( R_b \) to provide \( (n - 2) \) new functions. The total number of functions attainable by virtual ORing is given by

\[
\text{functions} = (n - 1) + (n - 2) + \cdots (n - (n - 1)) = (n - 1)!. 
\]

**Total Functions**

All of the functions obtained from the resistors and from ORing transistors are simultaneously available. Changes on input connections result in more functions, as described in the following.

Because each input switch is best realized as a constant-current switch, it is immaterial whether an input appears on the left or right side. Therefore, by interchanging any input variable and the reference, the output functions can reflect the effect of inverted inputs. Each one of the \( 2^n \) combinations of the input variables can be applied effectively to the gate by connections to left- or right-side switch inputs. However, half of these connections would result in duplicated outputs. Thus, \( 2^{n-1} \) input combinations will result in different output functions. The total number of functions available from a gate is given by

\[
F = (2n + (n - 1))2^{n-1}
\]

where the \( 2n \) term represents one function per resistor, the \( (n - 1)! \) term is a result of virtual ORing, and the \( 2^{n-1} \) term results from changing input connections to the switches.

Any \( n \)-input gate can also realize any function of an \( (n-1) \)-input gate by connection of the extra input to constant 1 or 0, depending on whether it is a left or right input.

**Limitations**

The normal limitations encountered in threshold-logic gates of this type are controlling the fan-in in combination with the threshold setting to allow for sufficient worst case margins and noise immunity. Clamping is also of concern to prevent saturation for high-speed operation.

In the original gates (which provided complementary outputs), the two sum points were connected with cross-coupled diodes for clamping [2], [3]. In Fig. 1(a), for example, with \( R_f \) and \( R_b \) equal, when one sum point is at or near its extreme low limit, the other is at its high end, and vice versa; thus one of the two diodes can conduct to equalize the two sum point potentials. This technique guarded against saturation of any transistors, and limited signal swings to values reasonably close to those immediately above and below the threshold. Because this symmetry is destroyed in the multifunc-

\(^1\) Otherwise \( R_a + R_b \) would always be high.
tion gates, different clamping arrangements are required. Negative clamping is relatively easy; a clamp source feeding emitter-followers is connected to each sum point [5], [6] to prevent saturation of the differential switch transistors. Positive clamping, if necessary, is generally accomplished with a diode and current switch. The current is routed through the sum resistor if its potential gets too high [6]. The signal swing about the reference is proportional to the total resistor for that function. Thus, it is lowest for OR and NAND functions and highest for AND and NOR functions for any given size gate.

As an example of signal swings, it may be assumed that \( R_u = 600 \, \Omega \) and \( V_{ps} = -4 \, \text{V} \) (these values correspond to unit current of about 2 mA). Then, for a five input gate, the swings are as follows (values of \( R_f/R_u \) are obtained from the curves of Fig. 4):

- **OR:** \( \Delta V = (0.22)(600 \, \Omega)(2 \, \text{mA}) = 264 \, \text{mV} \)
- **MAJ:** \( \Delta V = (0.4)(600)(2) = 480 \, \text{mV} \)
- **AND:** \( \Delta V = (2)(600)(2) = 2400 \, \text{mV} \).

The noise immunity is generally a little more than half of the signal swing; if worst case margins are accounted for, the OR function for the five-input gate might be in the order of 100 mV. The curves of Fig. 4 in effect show the variation of noise immunity with function and fan-in. For example, the \( T_i = 1 \) curve goes from \( R_f/R_u = 0.4 \) for \( n = 3 \) to \( R_f/R_u = 0.12 \) for \( n = 9 \).

**Multifunction Gate Designs**

The concepts described thus far are applied below to four practical examples: adder, three-addend adder, general parity circuit, and majority voter with error signal.

**Adder**

Fig. 5(a) shows a conventional threshold-gate full adder, as well as its well-known logic symbol. Fig. 5(b) shows a full adder utilizing the freedom of multifunction design. The left-hand summing resistor sums the three inputs, as described above, to derive \( C_0 \). \( C_0 \) drives a double-weighted current switch (as before), which now sums on the same right-hand summing resistor shared by the original three switches—the 3-out-of-5 value resistor \( 2 \, R_u/5 \). This resistor then provides the sum. \( C_0 \) is derived from \( C_0 \) [5], [6].

The multifunction design provides a savings in current switches as compared to the conventional threshold-logic design, with attendant savings in power and connections. Speed is about the same because two switch delays are traversed before the sum output is stabilized.

**Three-Addend Adder**

A three-addend adder threshold-logic design, suggested by Winder [5], is shown in Fig. 6(a). It has, of course, the three inputs to be added, as well as two carry inputs and two carry outputs. The multifunction design is shown in Fig. 6(b). Two new techniques are used simultaneously—deriving two functions from one summing side and a third, the sum output, from the other side.

The original logic design is directly translated into the schematic. The two upper gates calculate the 2/5 and 4/5 functions. Because the 2/5 sum resistor \( R_1 \) is smaller than the 4/5 sum resistor, its voltage is added to a resistor \( R_2 \) so that \( R_1 \) and \( R_2 \) provide the 4/5 value.
These outputs sum double-weighted modules, as before, which sum on $R_s$, the $5/9$ sum resistor of the output gate. The savings in this circuit are even greater than in the full-adder example because the five-input cluster is used once instead of three times.

**General Parity Circuit**

The concept of the adders (which can also be considered as three-bit and five-bit odd parity circuits) is generalized in Fig. 7. Fig. 7(a) shows the threshold-logic realization of a parity circuit that minimizes delay. Fig. 7(b) shows the multifunction realization. The values of the resistors are given in Table I.

**Majority Voter with Error Signal**

Fig. 8 shows a further application of the multifunction design [5]. The circuit in Fig. 8(a) is a standard threshold-logic design providing a majority output and an error indicator. Fig. 8(b) shows the multifunctional design that provides the same functions. The left-hand summing resistor provides a **NOR** function—a high signal *only* if all inputs are low. The right-hand side has the conventional 2-out-of-3 resistor to provide the majority output, plus a resistor that provides the **AND** function—a high signal *only* if all inputs are high. By virtual ORing the **AND** and **NOR** outputs because emitter-followers are available, an error signal is obtained—this signal is high only if all the inputs agree.

**Summary and Conclusions**

Instead of using the normally complemented outputs of a family of integrated threshold gates, resistors are specified that result in grossly different functions for each side of the gate. In fact, a single side of the gate can provide several functions of the input variables simultaneously. A combination of these techniques applied to conventional threshold-logic designs has demonstrated very large improvements in power, components, and connections (and therefore chip area).

The circuits shown were initially very advantageous for threshold logic (when compared to Boolean logic gates). Previous studies [4], [5], [7] have shown improvements of 3 to 1 in power and complexity for symmetrical function realization (adders, parity, etc.) with the regular integrated threshold-logic circuits.
For any given function, the multifunction circuit technique uses the same number of emitter-followers (one per output) and summing resistors. However, the number of current switches and resultant power and connections is significantly reduced. Both power and connections are proportional to the number of current switches. Table II compares multifunction threshold logic and conventional threshold logic for four examples; savings of from 2 or 3 to 1 are obtained. These figures indicate that special functional chips using these techniques should be considered. The basic principles have already been proven in integration, and the designs are simple. Such multifunction threshold-logic chips as arithmetic units, multipliers, parity arrays, and majority voter arrays can easily be made compatible with conventional ECL logic and yet provide improved performance.

In general, the two summing resistors can be driven by different variables, some of which are common to both sums. The adders and parity circuits exemplify this principle.

TABLE II

<table>
<thead>
<tr>
<th></th>
<th>Number of Current Switches or Number of Connections</th>
<th>Relative Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Threshold Logic (T/L)</td>
<td>Two-Addend Adder</td>
<td>7</td>
</tr>
<tr>
<td>Multifunction Threshold Logic MF (T/L)</td>
<td>Three-Addend Adder</td>
<td>17</td>
</tr>
<tr>
<td></td>
<td>Eight-Bit Parity Circuit</td>
<td>12</td>
</tr>
<tr>
<td>MF T/L</td>
<td>Majority Voter/Error Signal Circuit</td>
<td>3</td>
</tr>
<tr>
<td>T/L</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MF T/L</td>
<td></td>
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</tbody>
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