RULES FOR INPUT EQUATIONS FOR ALL FLIP-FLOPS

<table>
<thead>
<tr>
<th>FF</th>
<th>On Map</th>
<th>On $\overline{Q}$ Half (for 1)</th>
<th>On Q Half (for 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>D</td>
<td>0 0 0</td>
<td>1 0 1</td>
</tr>
<tr>
<td>T</td>
<td>T</td>
<td>1 0 0</td>
<td>0 1</td>
</tr>
<tr>
<td>J-K</td>
<td>J</td>
<td>1 0 X</td>
<td>X X</td>
</tr>
<tr>
<td></td>
<td>K</td>
<td>X X 0</td>
<td>0 1</td>
</tr>
<tr>
<td>R-S</td>
<td>R</td>
<td>0 X 0</td>
<td>X 1</td>
</tr>
<tr>
<td></td>
<td>S</td>
<td>1 0 X</td>
<td>0 0</td>
</tr>
<tr>
<td>RST</td>
<td>R</td>
<td>0 X 0</td>
<td>$\overline{X}$</td>
</tr>
<tr>
<td></td>
<td>S</td>
<td>$\overline{Y}$ 0 X</td>
<td>0 0</td>
</tr>
<tr>
<td></td>
<td>T</td>
<td>$\overline{Y}$ 0 0 X</td>
<td>0 0</td>
</tr>
</tbody>
</table>

On all maps $x$'s are plotted as $X$'s.

are to be 1 (or 0), and the same is true about $a_1$, $a_2$, and $a_4$.

The results, in fact, have been reported earlier by Biwas.\(^6\) He has derived general rules for the input equations for the $D$, $T$, $J-K$, R-S, and RST flip-flops. The rules, in a tabular form, are reproduced here.

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Comments on "Basic Properties and a Construction Method for Fail-Safe Logical Systems"

The paper by Mine and Koga\(^5\) appears to have some unstated assumptions and inconsistencies which affect the validity of their claim to have presented "an effective method of logical design for fail-safe systems."

The basic premise is that if outputs of elementary Boolean functions fail in only one way (stuck-at-0 or stuck-at-1 exclusively) then one can construct combinations of these functions whose terminal output will similarly fail in the same way.

An unstated assumption appears to be that an output failure of a preceding stage is logically equivalent to an input failure of a following stage. For example, when 0 is at electrical ground, an open or a shorted-topower input to an AND is equivalent to the preceding stage output stuck-at-1, and a shorted-to-ground input is equivalent to the preceding stage output stuck-at-0. Similar reasoning applies to OR input failures. But the assumption is not valid when an output can fail in only one way, for some possible input failure of a following stage is not being considered.

The terminal logic of one of their examples is shown in Fig. 1\(^5\). In this example, all outputs are supposed to fail-safe at 0. The $X_1$, $X_2$, and $X_3$ inputs are assumed to realize a non-failed-0 or a failed-safe-0 at 1, 0, and 1, respectively. But if the $f'$ input should fail-open, the output of the following AND will be equal to the $X_3$ input, causing the terminal output to become a non-fail-safe 1. If open inputs can occur, the method does not result in fail-safe logic.

On the other hand, if the unstated assumption was that only outputs can fail, the method is valid but inconsistent with the remainder of the paper. Section V illustrates several two-input RTL NOR circuits and gives a truth table where the input resistors are assumed to fail-open only.

Section V further erra with the "single failure assumption." If we redundantly parallel input resistors which can only fail-open, then the failure of either is undetectable. Hence when one resistor fails it will not be replaced, and the failure of the other will then force the circuit into a non-fail-safe condition. Paralleling resistors may extend the mean time between failures but does not result in a fail-safe circuit. Similar remarks apply to the parallel and series redundancy of the output transistors.

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Authors' Reply\(^3\)

In Theorem 3, it is clearly stated that the fail-safe output of a basic function is severely restricted by the failed output of the preceding basic functions (though two IF's in the statement of Theorem 3 should be IF's). It is obvious, as a matter of course, that a single failure of an element in a logical circuit may cause different effects on its following logical functions. It should be noted here that we do not deal with types of internal failures of logical circuits but with outputs of logical functions being restricted by their following logical functions. If open inputs to the terminal logic shown in Fig. 1 of Mr. Foster's comment are allowed, then the conditions in Theorem 3 are not satisfied anymore. This apparently does not cause any inconsistency in our paper\(^1\). Examples of fail-safe NOR circuits shown in Section V are illustrated for the construction of fail-safe logical systems only with NOR circuits. This should have been noted in our paper.

The short failure rate of the input resistors is neglected because it may be assumed to be far less than the open failure rate. We should modify the fail-safe logical circuits according to the various field data. This may be the next step and we have shown in our paper the circuits as a basic concept.

We do not consider in our paper failure detection problem, as is noted in the conclusion. This is a future problem which we are going to consider. Consideration of the mean-time-between-failures will be required also for practical applications in the future. Which is more important, fail-safe construction or good MTBF? It depends upon the requirements.

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\(^1\) Manuscript received January 22, 1968.

\(^2\) Mine and Koga, Example 5 and Fig. 2, pp. 282-287.

\(^3\) Manuscript received February 13, 1968.