Horizons in Guidance Computer Component Technology

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Abstract—An extensive survey of logic and memory component manufacturers conducted by the NASA Electronic Research Center and the industry has resulted in estimates of the state-of-the-art of components available to designers of on-board guidance and control computers for long-term deep-space missions for the 1970–72 period. The vehicle for the survey were the mission requirements for the synchronous satellite, lunar orbiter, Mars orbiter, and Jupiter fly-by solar probe missions.

Index Terms—Bipolar LSI, component selection, component survey, computer hardware requirements, computer hardware technologies, guidance computer requirements, large-scale integration, memory technologies, mission analysis, MOS (metal-oxide semiconductor), on-board aerospace computer components, semiconductor logic circuits, semiconductor logic technologies.

INTRODUCTION

The selection of components for the prototype of a next-generation on-board modular guidance and control computer for long-term deep-space applications with existing and future launch vehicles is considered in this report [1]. As the first step in the component selection process, the NASA Electronics Research Center and the industry surveyed the state-of-the-art in the semiconductor logic circuit and memory component technologies. Those considered promising for the implementation of on-board guidance and control computers for long-term deep-space missions in the 1970–72 period were given special consideration.

The survey focused on computer requirements for several specific long-term space missions, including the Jupiter fly-by solar probe mission. Of course, this mission is beyond the state-of-the-art relative to computer life, size, and power, but design problems typical of those to be expected in the design of on-board guidance and control computers for long-term deep-space missions were generated as part of the study. The survey resulted in recommendations for the logic and memory component technologies to be applied in the design of a 1970–72 prototype of such a computer.

Advances in semiconductor and memory technologies occupy important roles in the continuing progress in digital computer design. The advent of large-scale inte-


The authors are with NASA Electronics Research Center, Cambridge, Mass.

1 S. Polenger and B. DeRose, United Aircraft Corp. Systems Center, personal communication, November 15, 1967.
solar radiation is composed of two components—the solar flare and the solar wind particles. The frequency, intensity, and duration of flares are of a magnitude which does not represent a serious hazard to the equipment of the spacecraft, with the possible exception of the low-energy component. This component could damage the thermal control coatings. The Earth-trapped radiation is not a problem since the transit time through the radiation field is short. Jupiter’s trapped radiation belts are of sufficient magnitudes and energies to cause damage to certain types of semiconductor circuits [3]. Shielding against the high-energy nuclear particles trapped in Jupiter’s magnetic field does not seem to be a satisfactory solution. It is assumed that the radiation belts of Jupiter follow the Earth-type configuration. The most probable value of magnetic field around the planet is 1 gauss at a distance of 3 Jupiter radii. At this field strength experimental evidence indicates that the radiation field most probably consists of electrons in the energy range of 1 to 100 MeV. An electron flux scaling factor of $10^8$ then seems appropriate in estimating Jupiter’s environment from a knowledge of Earth’s environment. The proposed trajectories could, therefore, subject the spacecraft to 3 to 48 hours of 1-MeV electron flux rates of $10^8$ e/cm²·s and 80-MeV proton flux rates of $10^7$ p/cm²·s.

The thermal environment imposed on guidance and navigation system components is dependent on the skin temperature of the vehicle in which the system is mounted. The skin temperature, in turn, depends on the ambient condition, the trajectory-sun relationships of the mission, and physical characteristics of the space vehicle. Representative calculations of anticipated ambient thermal environments clearly indicate that an environmental control system is needed.

The mission time requirement for navigation varies from 6 hours for the synchronous satellite to 436 days for the Jupiter fly-by. This indicates that requirements on component lifetime vary by about 2000 to 1.

Examples of less critical environmental requirements include linear acceleration and pressure. All of the missions employ flight profiles which contain two periods of linear acceleration—launch and boost toward Earth parking orbit and transfer and mid-course maneuvers. All existing and future launch vehicles will deliver maximum linear acceleration during launch and boost. The ambient pressure environment ranges from a maximum of 1 atmosphere to a near vacuum. Because of the relatively short time of flight through the Earth’s atmosphere the major portion of the mission is accomplished under vacuum conditions. This pressure environment is acceptable, and therefore there is no need for pressurized compartments for the components.

**Computer Requirements**

Computer memory size, word length, and speed requirements for each phase of the four missions have been estimated by means of computer simulations [4]. These estimates have assumed a single-address, serial-operation machine. Execution of extensive diagnostic and correction routines and reconfiguration of the modular computer would certainly modify these estimates.

It has been assumed in the development of the computational requirements for boost and injection into parking orbit that the boost vehicle dynamics are the same for all the vehicles considered. Also, it has been assumed that the guidance system requirements for boost and injection are independent of the mission objective after the parking orbit phase of the flight. Fig. 1[4] summarizes the computational requirements for system accuracies from 1 to 10 ft/s at injection by computer functions. Fig. 2[4] shows required memory capacity, speed, and word length as a function of accuracy. It should be noted that speed is the most sensitive parameter. Fig. 3[4] depicts the memory capacity used in each phase of the four missions, the magnitude of memory not presently in use but required for future phases, and also the total memory requirements for each phase.

As each mission progresses, the total memory requirements decrease although the memory actively used shows both decreasing and increasing trends. However, a marked decrease in computational speed requirements is shown as the mission progresses. Finally, Fig. 4[4] shows the total memory requirements for each mission as a function of time.

Maximum memory capacity required is 12 800 words and a maximum instruction speed of 150 000 instructions per second for the boost and injection phase of the missions where an ADD is considered an average instruction. A 15-to-1 variation in speed occurs over the duration of the mission. To meet this instruction speed it is assumed that a memory READ-WRITE cycle time of 2 μs is needed.

The word-length requirements are determined, for the most part, by navigation requirements and vary from 16 to 32 bits. However, computational loads favor a long computer word rather than a short word as depicted in Fig. 1.

**Suitable Logic Component Technologies**

A survey of the state-of-the-art of computer logic components was undertaken by the NASA Electronics Research Center[3] and the industry. The survey results were extrapolated to provide an estimate of the state-of-the-art of logic components circa 1970–72 which will be available to designers of on-board guidance and control computers for long-term deep-space missions. Specific missions were selected to provide performance specifications representative of many long-term space missions. Some specifications were still incomplete, e.g.,

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[3] ERC representatives included members of the Guidance and Control Computer Branch of the Guidance Laboratory and members of the Qualification and Standards Laboratory.
Fig. 1. Computational requirements for injection into 100-nmi parking orbit.

Fig. 2. Computational requirements for injection into parking orbit.

Fig. 3. Memory requirements.

Fig. 4. Memory requirements versus time.

### Table: Computations and Word Lengths

<table>
<thead>
<tr>
<th>Computer Function</th>
<th>10-f/s Injection Accuracy</th>
<th>5-f/s Injection Accuracy</th>
<th>1-f/s Injection Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input/Output</td>
<td>300/70 (1)</td>
<td>3000 (5)</td>
<td></td>
</tr>
<tr>
<td>Prelaunch Alignment</td>
<td>(2)</td>
<td>(2)</td>
<td>(2)</td>
</tr>
<tr>
<td>Prelaunch Checkout</td>
<td>(2)</td>
<td>(2)</td>
<td>(2)</td>
</tr>
<tr>
<td>In-Flight Self Test</td>
<td>470/81 (1)</td>
<td>470</td>
<td></td>
</tr>
<tr>
<td>Attitude Computation</td>
<td>435/63 (24)</td>
<td>28 400</td>
<td></td>
</tr>
<tr>
<td>Guidance Computation</td>
<td>650/80 (21)</td>
<td>2600</td>
<td></td>
</tr>
<tr>
<td>Vehicle Control</td>
<td>460/70 (16)</td>
<td>9200</td>
<td></td>
</tr>
<tr>
<td>Mission Commands</td>
<td>500/100 (1)</td>
<td>5000 (3)</td>
<td></td>
</tr>
<tr>
<td>and Timing</td>
<td>660/104 (1)</td>
<td>2000</td>
<td></td>
</tr>
<tr>
<td>TOTAL</td>
<td>3957/621</td>
<td>47090-55 090</td>
<td></td>
</tr>
</tbody>
</table>

(1) Use available word length.  
(2) Overwritten at launch.  
(3) Perform as required.  
* Including sign position.

### Graphs:

- **Fig. 1:** Computational requirements for injection into 100-nmi parking orbit.
- **Fig. 2:** Computational requirements for injection into parking orbit.
- **Fig. 3:** Memory requirements.
- **Fig. 4:** Memory requirements versus time.

### Table: Mission Phases

<table>
<thead>
<tr>
<th>MISSION PHASE</th>
<th>Jupiter Fly-By</th>
<th>Synchronous Satellite</th>
<th>Lunar Orbiter</th>
<th>Mars Orbiter</th>
<th>Word Length</th>
<th>Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Present Phase</td>
<td>Future Phases</td>
<td>Total</td>
<td>Present Phase</td>
<td>Future Phases</td>
<td>Total</td>
</tr>
<tr>
<td>1) Boost and Injection to Parking Orbit</td>
<td>5000</td>
<td>7800</td>
<td>12 000</td>
<td>5000</td>
<td>3200</td>
<td>8200</td>
</tr>
<tr>
<td>2) Parking Orbit and Transfer Injection</td>
<td>4300</td>
<td>6600</td>
<td>10 900</td>
<td>4300</td>
<td>2000</td>
<td>6300</td>
</tr>
<tr>
<td>3) Transfer Orbit and Corrections</td>
<td>8100</td>
<td>1600</td>
<td>9700</td>
<td>3900</td>
<td>1200</td>
<td>5100</td>
</tr>
<tr>
<td>4) Terminal Maneuver</td>
<td>4300</td>
<td>4300</td>
<td>4300</td>
<td>4300</td>
<td>4300</td>
<td>8700</td>
</tr>
<tr>
<td>5) Orbital Navigation</td>
<td>7600</td>
<td>7600</td>
<td>7600</td>
<td>7600</td>
<td>7600</td>
<td>16-30</td>
</tr>
</tbody>
</table>

**MOS Versus Bipolar Technologies**

The principles of the MOSFET (metal-oxide semiconductor field-effect transistor) were patented by Lilienfeld and Heil more than 13 years before the bipolar transistor was invented. In the mid-1940's, these principles were further explored by Pearson and Shockley, but this work was overshadowed by the concurrent discovery of the bipolar transistor. The bipolar transistor...
was considerably less sensitive to surface effects than the MOSFET. It could be fabricated with germanium by the crude technology then available, and so bipolar became the dominant technology. Today, most bipolar integrated circuits are designed using the techniques [6] of Fig. 5. An \( N^+ \) well is diffused into a wafer of \( p \)-type silicon. An \( n \)-type film is epitaxially grown, into which is diffused a \( p \)-type isolation region, a \( p \)-type base region, and an \( N^+ \) collector region. The size is approximately 40 square mils. The semiconductor industry has an extensive experience and a large investment in the bipolar technology.

It was not feasible to manufacture MOSFET's until the development of the planar process in the early 1960's. The early devices were subject to charge migration which caused gross changes in operating parameters and deterioration of the \( p-n \) junctions. Most of the MOS devices currently manufactured are of the \( p \)-channel enhancement mode type of Fig. 6. The \( p \)-channel devices are somewhat easier to manufacture because of the same physical phenomenon that causes \( p-n-p \) planar devices to be easier to fabricate than \( p-n-p \) silicon planar devices. The \( p \)-channel device is fabricated by starting with an \( n \)-type substrate into which, significantly, only a single \( p \)-type diffusion is made. The manufacturing process requires about 35 steps and the resulting MOS transistor occupies about 2 square mils of silicon.

The complementary MOS circuitry offers several advantages over circuitry implemented with \( p \)-channel devices, e.g., it is far more tolerant to charged particle radiation damage. Complementary arrays will appear on the market during the 1970's since a major semiconductor manufacturer is committed to market complementary MOS arrays for memory applications by 1970. These arrays will contain several hundred bits of scratch-pad memory including all address, decoding, and selection electronics. However, complementary arrays are difficult to fabricate in either technology, and so for the 1970–72 period it was decided, from reliability considerations, that transistors should be all of one type, i.e., all \( p \)- or all \( n \)-type MOS, or all \( p-n-p \) or all \( n-p-n \) bipolar transistors.

It should be noted that MNS (silicon nitride replaces silicon dioxide as the gate insulator) devices exhibit more tolerance to radiation damage than present MOS devices. However, MNS devices are not currently available and MNS arrays are not expected to become available until the middle to late 1970's and so will not be available in the desired period.

In the case of deep-space missions, reliability is weighed heavily in any hardware selection trade-off study. It was estimated that the bipolar technology is more likely to yield more reliable circuits, at least in the 1970–72 period, because of the oxide-interface-channel reliability problems of the MOS. That is, for equal areas of silicon and equivalent control of cleanliness of fabrication conditions, the bipolar transistor would be the more reliable. The MOS can be made with smaller areas and so may have greater ultimate reliability, although the appearance of some new small geometry bipolar devices could threaten the size advantage of the MOS.

The bipolar technology is more advanced than the MOS (more experience has been accumulated) and so it also represents the more conservative selection for the specified time period. The bipolar technology was selected as the processing technology for the basic, large-scale arrays which will be used to implement the computer design.

**Discretionary Versus Fixed Interconnections**

Large-scale arrays are characterized at this time by high fixed cost and turn-around time. These costs can vary from thousands of dollars to tens of thousands of dollars, and design times can vary from weeks to months. The fixed costs must be added to the cost of actually fabricating and testing the LSI's (large-scale integration), and these additional costs can have a significant impact on the cost of the final packaged logic circuit. One hope for achieving economical LSI is to find application areas where the market requirements are sufficient to justify the initial expense, e.g., if a number of users can pool their requirements and so develop only a limited number of arrays. This approach might be feasible in special situations, e.g., if the set of users are the NASA on-board guidance and control computer designers.

A formidable problem is that of achieving high yields on these large arrays, although as a practical matter the number of leads feasible on a small package will limit the size of many arrays. The fixed-interconnection approach allows the array size to grow as advances in technology permit higher yields over larger areas. This approach implies a series of evolutionary steps. Most semiconductor manufacturers would prefer to help their present volume customers convert and update their present volume systems while retaining existing manufacturing procedures for the large arrays. This approach
seems to have a practical limit of around 150 gates for a 2.0-inch wafer where the limit is set by considerations of average yield. Few semiconductor manufacturers are interested in marketing small quantities of custom large-scale arrays.

As an example of the current direction of planning for the circa-1970 state-of-the-art, a major manufacturer plans to be marketing 200-gate, fixed-interconnection bipolar arrays by 1970. An LSI wafer which is a cellular matrix of identical networks of four 3-input gates capable of arbitrary interconnections is provided. Independent internal interconnections for each cell are provided with a first-level metallization, and the cells are then interconnected by a second-level metallization. The size of these arrays is limited by the yield obtainable. However, the technique is currently available.

Discretionary wiring is another approach to large-scale integration. At least three manufacturers are currently committed to the development of a capability for discretionary wiring. The semiconductor manufacturer uses a fixed but large array of logic circuits and he concedes that after fabrication there will be faulty circuits within the array. The final interconnection patterns are programmed to avoid use of these faulty circuits. LSI complexity is then limited by power dissipation and wafer dimensions. A unique set of interconnection masks is required for each wafer, and so if this system is to be economical, the costs of mask production and wafer probing must be reduced to a minimum.

A major semiconductor manufacturer plans to provide quick turn-around time by developing a full spectrum of design automation [7]. A wafer of 5 input NAND (NOT-AND), TTL (transistor–transistor logic) gates is automatically probed and the location of each electrically good gate is recorded by a computer. The computer then generates a code which provides input information to automatic mask-making equipment. It is estimated that 500- to 1500-gate (1.5 mW per gate) LSI configurations will be furnished with a minimum purchase order of about 50 identical circuit function wafers. The wafers will all have different wiring interconnections though they all perform identical logic functions and are tested to identical final specifications. The design automation system is due for completion by Spring 1968 and should be operational for industrial orders before mid 1968.

It is clear that use should be made of the largest available semiconductor arrays to implement the computer design, but since universal “elements” will not be available, both discretionary and fixed off-the-shelf types of LSI’s will be needed. However, questions of reliability of the “one-of-a-kind” discretionary wired LSI’s have resulted in a cautious acceptance by NASA designers. But, if the requirements for discretionary wired arrays are to be reduced, then fixed array development programs must be initiated, especially if these arrays will not appear as a natural evolution of technology and other user requirements.

Logic Circuits

Fig. 7 illustrates some of the more common bipolar logic circuit approaches [8], namely, DCTL (direct coupled transistor logic), RTL (resistor transistor logic), DTL (diode transistor logic), TTL (transistor–transistor logic), and CML (current mode logic). Circuit structure varies for different levels of integration. For example, a TTL circuit built from discrete components differs from its monolithic integrated counterpart in the construction of the transistors, some of which can be convolved, thereby reducing the component count. Similarly, an LSI version of a TTL circuit would eliminate some of the stages required for drive purposes. A comparison of each logic type to evaluate its potential for integration into large-scale arrays which would be suitable for implementing the design of a long-term, deep-space, on-board guidance and control computer must include the following characteristics: speed (propagation time delay), noise immunity, fan-out, and power supply requirements. Fig. 8 is a summary of the results of a literature search for the characteristics of representative types of bipolar integrated logic circuits presently being manufactured. However, Fig. 8 does not reflect technology capabilities that are being or will be incorporated in future products. Fig. 9 does reflect technology capabilities which it is estimated will be incorporated in the 1970–72 production bipolar logic circuits.

Direct Coupled Transistor Logic (DCTL)

DCTL is extremely device-dependent and hence has limited fan-in and fan-out, is temperature-sensitive, and has low noise margins. The transistors are heavily driven into saturation since the base current is almost equal to the collector current. The transistors then accumulate a large stored base charge with a corresponding decrease in switching speed. Voltage levels are low (total output voltage change is only about 500 mV for silicon) and so noise can be troublesome. Transistors with a low $V_{BB}$ (for a given $I_b$) will “hog” most of the available base current with the possibility that some of the transistors may not be driven into saturation. Hence, silicon transistors suitable for DCTL must have very close control on uniformity of input characteristics, as large a differential as possible between $V_{BE}^{(sat)}$ and $V_{CE}^{(sat)}$, a large $h_{FE}$, and a small storage time. It is clear, therefore, that satisfactory large-scale bipolar arrays of DCTL logic circuits would be very difficult to fabricate.

Resistor Transistor Logic (RTL)

If the DCTL circuit is modified by placing resistors in series with the bases, then the resulting circuit is often referred to as RTL. The RTL NOR (negative NAND) gate has relatively slow transient response, particularly if the transistor is driven heavily into saturation. Semiconductor manufacturers have decided not to produce RTL in large-scale arrays because of its ineffi-
Fig. 7. Logic circuits. (a) DCTL (direct coupled transistor logic). (b) RTL (resistor transistor logic). (c) DTL (diode transistor logic). (d) TTL (transistor-transistor logic). (e) CML (current mode logic).

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Available Degree of Integration (circuits/chip or circuits/wafer)</th>
<th>Speed (MHz)</th>
<th>Propagation Delay (ns)</th>
<th>Power (mW)</th>
<th>Speed-Power Product (W·s×10^-12)</th>
<th>Noise Margin (mV)</th>
<th>Fan-Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCTL</td>
<td>Discrete</td>
<td>5 to 15</td>
<td>5 to 15</td>
<td></td>
<td>&lt;300</td>
<td>&lt;5</td>
<td></td>
</tr>
<tr>
<td>RTL</td>
<td>25</td>
<td>≤5</td>
<td>10 to &gt;30</td>
<td>≤5</td>
<td>50 to 300</td>
<td>80 to 300</td>
<td>≤5</td>
</tr>
<tr>
<td>RCTL</td>
<td>16</td>
<td>&gt;30</td>
<td>&lt;10</td>
<td>&gt;150</td>
<td>300 to &gt;800</td>
<td>300 to 500</td>
<td>&lt;25</td>
</tr>
<tr>
<td>CML</td>
<td>16</td>
<td>&gt;15</td>
<td>&gt;30</td>
<td>&gt;10</td>
<td>80 to &gt;1000</td>
<td>300 to &gt;500</td>
<td>5 to 10</td>
</tr>
<tr>
<td>DTL</td>
<td>35</td>
<td>1 to 5</td>
<td>10 to &gt;30</td>
<td>80 to &gt;1000</td>
<td>100 to &gt;1000</td>
<td>&gt;750</td>
<td>5 to 10</td>
</tr>
<tr>
<td>TTL</td>
<td>73 (fixed) 500 (discretionary)</td>
<td>5 to &gt;15</td>
<td>&lt;10 to &gt;30</td>
<td>10 to 50</td>
<td>&gt;1000</td>
<td>&gt;750</td>
<td>5 to 10</td>
</tr>
</tbody>
</table>

Fig. 8. 1967 state-of-the-art for logic circuits in production in 1967.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Available Degree of Integration (circuits/chip or circuits/wafer)</th>
<th>Speed (MHz)</th>
<th>Propagation Delay (ns)</th>
<th>Power (mW)</th>
<th>Speed-Power Product (W·s×10^-12)</th>
<th>Noise Margin (mV)</th>
<th>Fan-Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCTL</td>
<td>Discrete</td>
<td>5 to 15</td>
<td>5 to 15</td>
<td></td>
<td>&lt;300</td>
<td>&lt;5</td>
<td></td>
</tr>
<tr>
<td>RTL</td>
<td>30</td>
<td>≤5</td>
<td>10 to &gt;30</td>
<td>≤5</td>
<td>50 to 300</td>
<td>80 to 300</td>
<td>≤5</td>
</tr>
<tr>
<td>RCTL</td>
<td>20</td>
<td>&gt;30</td>
<td>&lt;10</td>
<td>&gt;150</td>
<td>300 to &gt;800</td>
<td>300 to 500</td>
<td>&lt;25</td>
</tr>
<tr>
<td>CML</td>
<td>20</td>
<td>&gt;15</td>
<td>&gt;30</td>
<td>&gt;10</td>
<td>80 to &gt;1000</td>
<td>300 to &gt;500</td>
<td>5 to 10</td>
</tr>
<tr>
<td>DTL</td>
<td>200 (fixed)</td>
<td>1 to 5</td>
<td>10 to &gt;30</td>
<td>80 to &gt;1000</td>
<td>100 to &gt;1000</td>
<td>&gt;750</td>
<td>5 to 10</td>
</tr>
<tr>
<td>TTL</td>
<td>200 (fixed) 1000 (discretionary)</td>
<td>5 to &gt;20</td>
<td>&lt;10 to &gt;30</td>
<td>1.5 to 50</td>
<td>40 to ≤1000</td>
<td>&gt;750</td>
<td>5 to 10</td>
</tr>
</tbody>
</table>

Fig. 9. Estimated 1970–72 state-of-the-art for logic circuits in production.
cient use of silicon area and its large propagation delay time. There seems to be no obvious reason to encourage the development of such arrays with NASA funding. If capacitors are placed across the input resistors then the minority-carrier storage time can be reduced, and so a portion of the speed is regained which was lost by inserting the device-equalizing resistors. Such a configuration is called resistor–capacitor–transistor logic (RCTL). The RCTL circuit is vulnerable to high-frequency noise, which is coupled to the base through a capacitor. The principal justification for the use of RCTL apparently is economy. There are no plans to use either RTL or RCTL circuits.

Current Mode Logic (CML)

CML is a high-speed, nonsaturating circuit which is capable of operating with small propagation delays. To eliminate the minority-carrier storage time, the transistor is prevented from going into saturation. Complementary outputs are available. Higher speeds obtainable with CML are offset by the increased power dissipation and increased component count. In any application where speed allows any of the three logic types to be used, CML will dissipate more power than either DTL or TTL. The minimization of power supply requirements is an important consideration in the selection of components for the computer and so the choice is narrowed to either DTL or TTL.

Diode Transistor Logic (DTL)

The DTL circuit has good noise margins, high fan-out, and moderate propagation delays. The noise immunity is increased over that of the DCTL configuration because of the voltage drops across the reverse biased output diodes. The reputation of discrete DTL circuits for reliable operation has been established by long years of user experience, and hence the rapid acceptance of integrated circuits in this configuration.

Transistor–Transistor Logic (TTL)

If the diodes D and D1 of the DTL circuit of Fig. 7 are replaced by the base emitter and base collector junctions of a transistor, respectively, then the circuit is called transistor–transistor logic. TTL offers a potentially higher-speed unit than DTL for a given power consumption with no attendant increase in integrated circuit design or manufacturing complexity. DTL and TTL integrated circuits are currently competitive for the implementation of computers with clock rates between 1 and 5 MHz. TTL stands alone with rates from 5 to 20 MHz.

In array form, both DTL and TTL will probably occupy approximately equal surface areas and differ principally only in the interconnection of the input transistor. For DTL arrays, the base and collector are shorted together and then connected to a positive voltage and one of the emitters is connected to the base of the second transistor. However, for TTL arrays all of the emitters of the input transistor are inputs, the base goes to a positive voltage, and the collector is connected to the base of the second transistor. Design and fabrication costs and reliability considerations, then, provide no clear choice between DTL and TTL arrays. However, TTL has potential for future improvement (see Fig. 7) in propagation delay time and power dissipation since the input is active as compared to the passive input network for the DTL. It was concluded that saturating TTL appears the most promising as the basic logic circuit for the large-scale arrays to be used to implement the computer design.

Memory Techniques

General Considerations

The primary consideration encompasses some of the characteristics desirable in a main memory for a guidance computer. A spaceborne or aerospace memory must be able to store information without error for extended periods of time and under adverse environmental conditions. Accordingly, for an advanced guidance computer reliability is a most important factor. Other important areas for comparison, which vary in importance, depending on the intended mission of the computer, are volatility, power consumption, speed, cost, volume, weight, temperature sensitivity, mechanical strength, and magnetic tolerance. These factors are interrelated and must be traded off against one another.

DRO Versus NDRO

The most common space-qualified destructive read-out (DRO) memory in existence today is the coincident-current ferrite core. Planar film DRO memories exist but are not in wide use in aerospace applications. After completion of a read cycle, the DRO elements are permanently disturbed so that the memory electronics must be reenergized to remagnetize the elements, thereby restoring the memory word.

Two general types of nondestructive read-out (NDRO) memories are available. In the first type, called read-only (ROM), the information is mechanically written by threading wires, punching holes, or cutting wires by some relatively permanent means. In the second type, electronically alterable, the information is written into the memory in a manner similar to the DRO memory. Reading is also similarly performed as in the DRO case, but the magnetic disturbance produced by the read current is self-reversible; that is, the element returns to its initial state. This removes the requirement of a restore cycle.

Since in most missions the computer program is stored in memory, where the loss of all or any portion of this program makes the computer inoperative, protection of the stored program under adverse conditions such as temporary power failure or excessive electrical transients is necessary.
Because the DRO memory must maintain on-line electronics capable of delivering write-current pulses, the possibility of temporary electronic malfunction may cause the alteration of information. However, the NDRO memory, whose program may be entered by means of auxiliary support equipment, or whose writing electronics may be disabled during a mission, is only capable of producing false read-current pulses caused by electronic malfunctions. An additional benefit of an NDRO memory is reduction in power consumption because the elements are self-restored and do not require electronic restoration. If the number of read commands is much greater than the number of write commands, as is usually the case, this saving in power is evident.

A third advantage of NDRO is speed. In DRO memories, a major portion of the read-write (R-W) cycle time is spent performing the write operation. The major limitation to cycle time in core memory systems is the inhibit recovery time; the sense amplifier must recover from the large write transient.

To make an overall evaluation of these two types of memory systems, the proven reliability of DRO core memories versus the advantages of NDRO devices must be traded off. Some of these advantages are proved; others are not. Most of the NDRO memory elements are still in the laboratory developmental stage.

Memory Technologies

Magnetic Cores

Magnetic cores are presently the dominant technology in spaceborne memory systems. Three major types of core memories now exist: linear select (2D), coincident current (3D), and a compromise [9] between coincident-current and linear-select organizations (2½D).

Linear-select memories are the most expensive form of memory organization because of the word-driver circuitry, but the fastest because more than the minimum switching current can be applied to the ferrite core to increase its switching time. Coincident-current (CC) memories are cheapest because less selection and addressing electronics are required, but these have the disadvantage of a long-inhibit recovery mode that limits the present speed of CC memory systems to a 1-μs R-W cycle time, and probably a limitation of 700 ns by 1970-1972.

The 2½D organization permits faster operation than a coincident-current memory and lower cost than a linear-select memory, and is the trend in commercial core-memory systems. Most of the major core manufacturers have plans to announce 2½D core-memory systems using 20/12-mil cores (OD=20 mils, ID=12 mils) by the end of the year, with cycle time ranging from 500 to 650 ns for memory modules of 8 to 16 K words having 24 to 36 bits per word.

Another trend is the use of wide-temperature lithium ferrite cores, rather than the manganese magnesium cores now in use. This is analogous to the relatively recent trend from germanium to silicon in the semiconductor area. The basic reason for this change is the improved temperature characteristic of the lithium ferrite core.

The emphasis in commercial core systems is in lower costs and faster cycle times, and all developments point in these directions. Although the above two factors are important to advance guidance computer programs, other important goals of NASA are reliability, low power, size, and weight.

A new packaging scheme just recently developed eliminates the center supports in core arrays so that it is now possible to stack 12 bits per inch, rather than the usual 8 bits per inch. The packaging densities available with cores are presently 1600 bits/in² because of the use of smaller cores (20/12 mils). The half-select currents needed for switching are 400 mA for a 1-μs memory cycle time with 30/18-mil cores. The above packing densities and current requirements compare very favorably with other technologies.

For space applications, it appears desirable to have a core that requires switching currents of less than 200 mA so that integrated circuit drivers can be used, and yet furnish a switching speed of 300 ns to make a 1-μs cycle time feasible. Research programs are in progress to develop low-current, wide-temperature cores, but with a goal of 3- to 4-μs cycle time.

There are many predictions that other technologies are to replace magnetic cores, but magnetic-core technology is so widespread and established that it is difficult for other technologies to replace it. The core suffers, however, from the limitation of only DRO operation, unless more sophisticated geometries are used such as the multiaperture devices (MAD) or Biax.

The multiaperture devices use the technique of two or more holes whose axes are parallel. By means of an appropriate pattern of conductor wires a flux pattern can be set up to give NDRO operation, although a prime current cycle is required after every interrogate pulse. A memory of this type is very expensive, and requires relatively intricate wiring and has severe temperature limitations. Two devices [10] using this technique are the transfluor and the Shmoo element. The currents required for these devices are high, 900 mA for clear and 550 mA for set, with a minimum read-modify-write time of 4 to 5 μs.

The Biax [11] is a block of pressed, square-loop ferrite material with orthogonal, nonintersecting holes. Read-out is derived from flux interference in the common volume of material between the holes. Binary state of the element is determined by polarity of permanent flux around the storage hole. Various operating modes are possible. A two-wire scheme operating in a ratchet-write mode is usually used. The Biax is capable of high-speed (20 MHz) read-out operation, but for a read-modify-write mode it is limited to about 5 μs.
Required write current is 360 mA. The Biax is temperature-sensitive because its $B-H$ loop is nonsquare and therefore extensive current compensation is needed. Its Curie temperature is 200°C. The usual application of Biax elements is in bootstrap operations, where the information is loaded on the ground with test support equipment and then operated in a read-only mode in flight.

The status of both the Biax and the Shmoo was reviewed in the course of the survey. No perceptible effort is presently being expended to improve either of these techniques, however, so that no significant improvements in materials or geometries can be expected by 1970–1972.

**Plated Wire**

This is a type of magnetic-film memory fabricated by plating a magnetic film on a wire substrate. A cylindrical film has advantages over planar films in having a closed flux path in the digit direction, thus requiring lower digit currents and a larger sense signal is obtained.

A 10 000-Å permalloy film is plated on a 5-mil beryllium copper wire. This wire serves as the plating substrate as well as the digit sense wire. The plating process applies a bias current down the wire to give a magnetic easy-axis circumferential to the wire. The magnetic material is electroplated on a continuously moving wire in a room environment.

Basically, two types of plated-wire memories are available, i.e., the strip-line technique [12] and the woven-wire approach [13].

In the strip-line technique, the word drivers consist of flat-metal strips placed over the digit wires. These word-drive straps are either returned under the digit wires or terminated in a ground plane beneath the digit wires. The digit lines are typically on 30-mil centers and the word straps on 50-mil centers, giving a packing density of 700 bits/in².

The second type makes use of a weaving process to fabricate the memory planes. The plated wire is woven into a matrix at right angles to insulated word-drive lines by means of a large automatic loom. The rest of the process is very similar to the strip-line technique. The woven wire provides a tighter magnetic coupling than in the strip-line approach, and also enables easier implementation of multiple turns in order to reduce the drive currents. It has more capacitative coupling, however, than the strip-line technique.

The plated-wire device is capable of both NDRO and DRO operation. For NDRO operation, the required drive currents for the strip-line version are $I_w=I_d=360$ mA and $I_d=40$ mA, with a worst-case sense voltage of 2.5 to 5 mV. Tolerances on all currents are 10 percent for a 0- to 50°C temperature range, without compensation of drive currents. With compensation, NDRO operation is feasible from $-10^o$ to $85^o$C. Equal read and write currents may be used, giving the plated-wire memories multiword organization capability and all the advantages of NDRO operation as previously described. Although the plated-wire organization is basically linear-select, because of multiword organizations, it is possible to minimize the number of digit drivers and sense amplifiers. With equal read and write currents it is also possible to simplify the word driver electronics.

For the woven-wire planes, the required currents are read 265 mA, write 500 mA, and digit 65 mA. The output voltage is 2 mV for a 50-ns rise-time, read-current pulse. Also, memory planes which require equal read and write currents are now available.

One large computer organization has announced use of NDRO plated-wire memories in a new series of computers with a capacity of 16 000 bytes (9 bits/byte) and a read–write cycle of 600 ns. Also, a fully qualified 1024-word, 24-bit-per-word plated-wire memory stack for a military program with a 2-μs R–W cycle is presently being developed. This memory has NDRO capability and uses equal read and write currents. Other programs with government agencies to develop woven-wire memory stacks ranging in size from 512 to 4096 words and with speed requirements of 2 μs or slower are in development. In addition, most of the companies visited have at least small plated-wire memory programs, even though their major effort may be in a different technology.

Although the plated-wire technology has many potential advantages, it is not without problems. The major problem is an aging effect, where it is found that NDRO properties of the plated wire deteriorate over a period of time. It is thought that the problem is caused by stress of the plated wire after plating or to copper migration from the beryllium substrate onto the thin-film plated film, which changes the film's magnetic properties. An additional problem is that of adjacent word disturbs, which is basically a creep, skew, and dispersion problem. This limits the packing density presently to about 700 bits/in² and the current tolerances in NDRO mode.

Extrapolations to 1970–1972 indicate an increase in packing density and reduction of drive currents compatible with the current-driving capabilities of integrated circuits by reducing the size of the beryllium copper wire from 5 mils to approximately 1 mil in diameter. Plated wires also are being designed for use in scratch-pad and fixed-memory applications, and thus have the potential advantage of use in all memory applications for a guidance computer for future long-term space missions.

**Planar-Magnetic Thin Films**

At present, planar films are used primarily in small high-speed control and scratch-pad memories. The past
10 years show slow progress in this film technology, which is handicapped by a number of difficult processing steps as well as an open-flux structure resulting in small sense signals and a tendency to demagnetize along the outer edges of the bit spot. These limit the thickness of the film and, thus, the output-sense signal. Other problems include dispersion, skew, magnetostriiction, and high-drive currents.

However, a thin magnetic-film NDRO element, such as the Bicore [14] or Quadrallory
d elements, exists and shows promise for use in NDRO main memory applications. The Bicore element is flight-qualified and is used in aerospace computer memory systems. The Quadrallory element is presently being incorporated in the Phoenix guidance computer system. In both of these applications, however, information is loaded into memory by test support equipment, and then operated in a READ-only mode in flight. In a READ-MODIFY-WRITE mode, present achievable cycle times are 7.5 μs, and high drive currents of 1.5 A for WRITE, 800 mA for READ, and 100 mA for DIGIT are needed. Densities are similar to those obtainable with planar thin films, 600 bits/in².

These elements consist of “soft” and “hard” magnetic layers. The soft layer can be subjected to relatively modest magnetic fields, whereas the hard layer must be influenced by a much larger field to cause a change in its magnetization. During WRITE operation a large field is applied to switch the hard film to the desired state. During READ, a smaller field is applied to the soft film to produce a signal output. The relatively un influenced hard film provides the restoring field to bring the soft film back to its original state, and this gives NDRO operation.

Recent developments by Pohm [15] at Iowa State University show promise for this device. Pohm has developed an element with a finite geometry with multturn word lines requiring 30 mA for READ and 80 mA for WRITE, with an increase in packing density of 10 over conventional thin-film arrays to ~800 bits/in². Since integrated circuits can easily supply this current by 1970–1972 it may be possible to have an all-integrated Bicore memory system. This small Bicore element has been shown to operate in a READ-MODIFY-WRITE mode of less than 500 ns in modest-size arrays, 128 bits.

The disadvantages of this approach are a) noncompetitive cost with core memories because of low yields and inability to make large arrays with uniform properties, b) small output signals, ~1 mV, and c) long-term “disturb” sensitivity.

Another development in the magnetic-film area is the multilayer film structure, in which two layers of magnetic film of similar composition are vacuum-deposited, first one and then a second, to enclose an inner conductor, the digit-sense wire. In essence, the element has a closed flux path in the digit direction but not in the word direction, and thus low-digit drive currents are possible, 15 to 20 mA. Although most of the effort at the present time is directed towards DRO multilayer film memories, an optimum space-memory element may be one that uses two different magnetic-film layers (different magnetic compositions), as in the Bicore element, but fabricated by use of the multilayer film technique. Such a structure possesses inherent NDRO properties based on a steering field that the hard film provides. This steering field restores the soft film back to its original state; therefore, the element has a higher magnetic tolerance and less sensitivity to noise than present-day devices.

**Etched-Permalloy Toroids**

In this technique [16], a permalloy sheet is etched in a pattern to give a matrix of toroidal-permalloy storage elements. A number of plating and etching processing steps is required to fabricate the conductors that serve as the drive and sense lines for the memory plane.

An 8 K-word, 30 bits per word, DRO aerospace memory using this technique is being developed. It has a 2-μs R–W cycle, a volume of 64 in³, power dissipation of less than 10 W, and it is operated in a linear-select mode. Low currents capable of being implemented by present-day integrated circuits are required for operation, \( I_g = 150 \text{ mA}, I_w = 120 \text{ mA}, \) and \( I_d = 50 \text{ mA} \).

Presently a 10³-bit NDRO mass memory is also being developed under contract to the Air Force, using this memory technique. It is a three-wire, coincident-current memory system using 23/17-mil toroidal cores. It has an R–W cycle time of 35 μs and an access time of 15 μs, and operates in an NDRO mode by using an RF-sensing scheme.

In summary, the permalloy-toroid approach requires a very large number of processing steps and interconnections. The elements consist of multilayer structures that have different chemical compositions, and the technology requires the conversion of KTPR from a photographic material to an insulating material. The permalloy material is very nonsquare and has a slow switching-time coefficient that limits its speed capabilities to ~2 μs. Its big asset is low drive requirements. The technique does not appear suitable for NDRO fast main memory systems. When low power, size, and weight are important, however, it shows considerable promise.

**Monolithic (Laminated) Ferrites**

The monolithic ferrite technique [17] is a batch-fabricated approach. The basic operations involved in fabricating a monolithic memory are doctor-blading, laminating and sintering, and conductor screening. The memory planes are fabricated in an array of 64 by 64
crossovers. Planes are fabricated by laminating three sheets of doctor-bladed ferrite. After sintering, the ferrite laminate shrinks to an overall thickness of 5 mils, with conductor spacing of 15 mils for a packing density of 4000 bits/in².

Two types of ferrite material are available for use in this technique: a) a high-current drive, fast-switching material (0.1×10⁻⁴ Oe-s), and b) a low-drive, slow-switching material (0.6×10⁻⁴ Oe-s) [17a]. Both materials have relatively low Curie temperatures (260°C), making temperature compensation of the drive currents beyond a range of 0 to 50°C necessary. The currents for the high-drive material are \( I_s = 440 \) mA, \( I_w = 110 \) mA, \( I_d = 35 \) mA, and for the low-drive material, \( I_s = 100 \) mA, \( I_w = 70 \) mA, \( I_d = 15 \) mA. Sense voltages are 5 to 10 mV for the high drive and 3 mV for the low drive.

Present operation of monolithic ferrites is confined to a DRO linear-select mode. The memory device possesses no inherent NDRO properties although various schemes are used to obtain NDRO operation.

Fabrication of the large memory arrays, 256 by 100, with acceptable yield and uniformity is necessary for the technique to compete favorably with other advanced memory techniques.

At the present time the fabrication of the large arrays is in the laboratory stage. By use of these 256 by 100 memory arrays it is possible to reduce significantly the number of required interconnections in memory modules. From a reliability point of view, the present method of connection from the drive circuitry electronics to the embedded conductor in the ferrite wafers needs investigation.

A research program is in progress in the industry, however, to develop MOS word-drive electronics for the low-drive ferrite material so that a fully integrated memory system may be feasible. Nevertheless, the monolithic ferrite technique does not appear promising for main memories for guidance application, where an NDRO element is desired and 2-μs or less R–W cycle times are needed. It may have application in large-capacity memory applications where size is of prime importance because of its excellent packing density, 4000 bits/in², and low-drive current requirements.

Integrated Circuits

For scratch-pad or high-speed control applications, there is little doubt integrated circuits [18] are to become the dominant technology in 1970–1972, replacing planar thin films currently in use. For a capacity of \( 10^6 \) bits, an R–W cycle time of 50 ns is feasible for bipolar integrated circuit arrays and an R–W cycle time of 150 ns for MOS arrays.

Although integrated circuits have been proposed for main memory applications, they are not being considered seriously because of their volatility and active element characteristic. The power required per stage is a serious problem when memories of large capacity are considered.

Arrays of 16 bits (bipolar) are available from several vendors and arrays of 64 bits are expected shortly. Power dissipation per bit is relatively high, 10 mW. An experimental scratch-pad memory (256 words, 72 bits with a 150-ns write cycle time) from small arrays of four words of 9 bits each on single 60 by 80-mil chips is available.

Other programs are being pursued to develop 1000-gate arrays. One program is concentrating on MOSFET arrays, another on bipolar, and a third on a combination of MOS and bipolar arrays where the decoding circuitry is bipolar and the memory elements are MOS.

Summary of Characteristics

A summary of characteristics for present state-of-the-art for main memory storage devices is detailed in Fig. 10 and a summary of an estimate of characteristics for main memory devices for 1970–1972 is illustrated in Fig. 11. It should be pointed out that the numbers in Figs. 10 and 11 are correlated; for example, the READ speed is a function of capacity, mode of organization, and READ current.

read-only Memories (ROM)

Although the main emphasis in the memory survey centers on main internal memories, a few words about the present technology of read-only memories appear in order. A read-only memory is one in which there is no electrical means of altering information. Memories using linear electrical coupling, \( R, L, \) and \( C \) arrays, nonlinear coupling, diode, transistor, nonlinear magnetic elements, and optical elements have been developed. ROM’s are used because they offer speed, size, and cost advantages over electrically alterable memories.

The most common ROM is the transformer type, one form of which is called the “core rope” [19] because of its physical resemblance to lengths of rope. The core rope consists of transformer cores threaded by a large number of word lines. The word lines either thread or bypass each transformer so that a “1” is represented by an output pulse and a “0” by the absence of a pulse when energized by a READ pulse. Address decoding is designed into the wiring structure and, thus, high bit densities (1500 bits/in²), including all electronics, can be achieved. Present efforts are directed at a variant of the transformer memory called a “braid” [20] which uses weaving with a loom as a means of manufacture to reduce the cost of fabrication.

A second type of ROM, holding considerable promise for use in 1970–72, is the LSI diode or transistor matrix. A silicon-on-sapphire (SOS) technology [21] giving densities of 10 000 to 50 000 bits/in² is available. This technique combines the active device properties and stabil-
**Summary**

The circuit complexities anticipated, the duration of the deep-space missions, general considerations of reliability, and the desire for low power, eliminated logic circuit technologies from consideration which will not be available in array form during the 1970–72 period. The chief contenders are the processing technologies by which silicon integrated devices are realized, i.e., the MOS and bipolar technologies. It is clear that use should be made of the largest available semiconductor arrays to implement the computer design, but since universal "elements" will not be available, both discretionary and fixed-interconnection off-the-shelf semiconductor logic circuits will be needed.

In the case of deep-space missions, reliability is weighed heavily in any component selection trade-off study. It was estimated that the bipolar technology is more likely to yield the most reliable semiconductor logic circuits, at least in the 1970–72 period, because of the oxide-interface-channel reliability problems of the

Fig. 10. Present state-of-the-art for main memory storage devices.

Fig. 11. Estimate of characteristics for main memory devices for 1970–1972.
MOS, DTL and TTL bipolar logic circuits are currently attractive and competitive for the implementation of computers with clock rates between 1 and 5 MHz. It is estimated that design and fabrication costs and reliability considerations will provide no clear choice between future DTL and TTL arrays. But, TTL shows promise for improved switching speed and power dissipation.

It is estimated that memory requirements would be a capacity of less than 10⁶ bits and a read-write cycle time of 2 μs. Memory technologies investigated were magnetic cores, plated wire, planar-magnetic thin films, etched-permalloy toroids, monolithic ferrites, and semiconductor integrated circuits. Both NDRO and DRO memory techniques could be used to implement guidance computer memory systems. NDRO techniques are less sensitive to electronic malfunctions and electrical transients, require less power, and are faster than DRO organization. However, NDRO memory systems are less tolerant of environmental conditions, e.g., temperature and drive current magnitudes.

Among the more promising technologies for general NDRO applications are the plated wire, elements of the Bicore multilayer type, and the Biwax. It is estimated that by 1970–72 reduced plated-wire drive current requirements will make feasible fully integrated memory systems. The NDRO properties of plated wire are currently a function of time and temperature, while adjacent word disturbs are a function of creep, skew, and dispersion. Elements of the Bicore multilayer variety with NDRO properties are flight-qualified for use in aerospace computers. The recent developments made by Pohm of Iowa State make this approach promising. Here “fine” geometry Bicore-like elements that require low drive currents are fabricated, and read-modify-write cycle times of 1 μs are achieved. Past space-memory programs have proven the Biwax technique, although discrete, to be highly reliable. It has sense voltages of about 10 times those obtainable with the plated-wire or Bicore technologies, and its packing density compares rather favorably with the densities achievable from other techniques.

As for DRO applications, the most likely memory technologies for a guidance and control computer for long-term deep-space missions are the magnetic-core, the plated-wire, and the multilayer magnetic-film elements. Extrapolation of current core technology indicates improvement in 3D and 2½D core organizations. As previously noted, the plated-wire device is capable of both NDRO and DRO operation. In the DRO mode, the tolerances on the environment and drive currents are more relaxed than in NDRO applications. The multilayer film technique offers a means of significantly reducing the number of interconnections in present magnetic thin-film arrays.

For scratch-pad or high-speed control applications, bipolar integrated circuit memories show much promise. This type of memory technology is compatible with large-scale integration (LSI) techniques, and offers the advantages of high reliability, high packing densities, and potential low cost.

In applications where an unalterable read-only memory is desired to guarantee integrity of information, the transformer-memory technique appears promising. This technique demonstrates proven reliability and is space-qualified for use in the Apollo guidance computer. The “braid,” a variant of the transformer memory technique, is presently being developed to reduce the cost of fabrication. A loom is used as the means of manufacture of the transformer array.

**Conclusions**

It is difficult to forecast the state of fast-moving fields, such as those of semiconductor devices and memory technologies, for a period from 3 to 5 years hence. It is even more difficult to suggest technological preferences for specific applications under the conditions of incomplete specification of the application, e.g., temperature and shelf operating life. However, it is possible to suggest most likely possibilities based on considerations of reliability and the present direction of technological development.

If the requirements for discretionary wired arrays are to be reduced, then fixed-interconnection array development programs must be initiated. Programs should be initiated early aimed at the study and achievement of devices to required specifications, radiation tolerance, and reliability. The goals of commercial programs are not aimed at all the ends needed here, and a special effort is required for research and development in these areas.

Magnetic cores are presently the dominant technology in spaceborne memory systems and will still be an important factor in DRO memory systems in the 1970–72 time period. However, it is believed that the potential advantages of batch fabrication, higher reliability, and minimum size, weight, and volume of other technologies will be realized. This is particularly pertinent for NDRO devices where the potential advantages of new technologies that are still in the developmental stage must be traded off against the proven reliability of the DRO core memories.

If the plated-wire memory technology is to achieve its potential, then the problems of aging and adjacent word disturb must be resolved. The adjacent word disturb problem presently limits packing density to 700 bits/in² and the drive current tolerances.

Also, by 1970–72 Bicore-like elements and multilayer structures fabricated by other techniques may be in production. In a multilayer structure reliability can be significantly improved by the reduction of the number of interconnections.

The industry trend to reduce the size of the ferrite core to 16/10 or 12/7 mils may allow an increase in core
memory speed and capacity. However, it appears improbable that the core size can be
significantly reduced below the 12/7-mil size because of the need to thread wires
through a 7-mil aperture.

RECOMMENDATIONS

Recommendations for the logic and memory component technologies to be applied in the
design of a circa 1970–72 prototype of a long-term, deep-space, on-board guidance
card and control computer for existing and future launch vehicles are as follows.

1) Semiconductor Logic Circuits: Bipolar, TTL saturating, one-transistor type, fixed-interconnection
arrays of about 100 gates/chip. Discretionary wired arrays when essential because of array size
or lack of development time.

2) Main Memory Technologies:
DRO: Magnetic core, plated wire, multilayer
NDRO: Plated wire, bicore multilayer, Biax RO: Transformer.

3) Scratch-Pad (High-Speed) Memory Technology:
Bipolar integrated circuit.

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