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Moore’s Law has been achieved through constant advances in manufacturing yield but also the development of dependability design techniques to keep the pace of the growing complexity of the computing systems. The objective of this Special Section is to cover issues related to the design, reliability, security and testing of integrated systems in the nanoscale era.

This Special Section consists of ten papers that have been selected to cover a wide spectrum of techniques, including the issues of low-power design, the test, the reliability, the security and trust of circuits manufactured with emerging technologies. Three papers are dedicated to design solutions for low-power devices. Three papers deal with reliability issues in memories, microprocessors and on-chip interconnections. Two papers discuss emerging solutions for the security of modern circuits. Finally, two papers propose novel solutions for the test of nanoscale integrated circuits.

With the aggressive downscaling of process technologies and the importance of battery-powered systems, reducing leakage power consumption has become a crucial design challenge for IC designers. In “An Exploration of Applying Gate-Length-Biasing Techniques to Deeply-Scaled FinFETs Operating in Multiple Voltage Regimes” by Tiansong Cui, Ji Li, Yanzhi Wang, Shahin Nazarian, Massoud Pedram, the authors present a device-circuit cross-layer framework to utilize fine-grained gate-length biased FinFETs for circuit leakage power reduction in near- and super-threshold operation regimes, by studying a 7 nm FinFET technology.

Low leakage is also explored in “Low-Leakage 3D Stacked Hybrid NEMFET-CMOS Dual Port Memory” by Marius Enachescu, Mihai Lefter, George Razvan Voicu, Sorin Dan Cotofana. The 3D stacked hybrid memory relies on Nano-Electro-Mechanical Field Effect Transistor (NEMFET) inverters to store data, and on adjacent CMOS based logic to allow for read/write operations, and data preservation. In this paper the authors assess the feasibility of a hybrid memory cell, and explore the design space of 3D stacked hybrid dual-port memory arrays which combine the appealing NEMFET properties, i.e., ultra-low leakage currents and abrupt switching, with the CMOS technology versatility.

A low-power programmable frequency multiplier operating in GHz frequency range is proposed in “A low-power frequency multiplier for multi-GHz applications” by Andreas Tsimpos, Andreas Christos Demartinos, Spyridon Vlassis, and George Souliotis. The architecture is based on the combination of a multi-segment programmable and power efficient phase interpolator with an edge combiner, in a 65 nm process with 1.0 V supply voltage offering a multiplication factor ranging from 1 to 8 with integer step.

Among the emerging technologies and devices for highly scalable and low power memory architectures, memristors are considered as one of the most favorable alternatives for next generation memory technologies. Nevertheless, some drawbacks including manufacturing process variability and limited read/write endurance, could risk their future utilization. In “Memristive Crossbar Memory Lifetime Evaluation and Reconfiguration Strategies” by Peyman Pouyan, Esteve Amat, and Antonio Rubio, the authors evaluate the impact of reliability concerns in lifetime of memristive crossbars.

“Comprehensive Reliability-Aware Statistical Timing Analysis Using a Unified Gate-Delay Model for Microprocessors” by Taizhi Liu, Chang Chih Chen and Linda Milor, proposes a framework to perform timing analysis of state-of-art microprocessors considering the impact of process-voltage-temperature (PVT) variations and the aging effect, including bias temperature instability (BTI), hot carrier injection (HCI), and time-dependent dielectric breakdown (TDDB). In this work, not only statistical timing analysis due to each wearout mechanism is studied individually, but also the performance degradation while all these wearout mechanisms happen simultaneously is analyzed.

In “Analytical Model for Resistivity and Mean Free Path in On-Chip Interconnects with Rough Surfaces” by Somesh Kumar and Rohit Sharma, the authors present a novel analytical model for calculation effective resistivity and mean free
path in on-chip copper interconnects. The closed form expressions are obtained from a generalized surface and grain boundary scattering approach that is combined with Mandelbrot-Weierstrass (MW) fractal function. 45 nm, 22 nm, 13 nm and 7 nm technology nodes have been considered for the analysis.

Security implications of on-chip voltage regulation on the effectiveness of various voltage/frequency scaling-based countermeasures such as random dynamic voltage and frequency scaling (RDVFS), random dynamic voltage scaling (RDVS), and aggressive voltage and frequency scaling (AVFS) are investigated in “Exploiting Voltage Regulators to Enhance Various Power Attack Countermeasures” by Weize Yu and Selcuk Kose. In particular, side-channel leakage mechanisms of different on-chip voltage regulator topologies are mathematically analyzed and verified with circuit level simulations.

IP-based design of Systems-on-chip (SoC) is enabling various new business models, which also bring inherently new security challenges for the protection of the intellectual property. In “An IP Core Remote Anonymous Activation Protocol” by Domenico Amelino, Mario Barbareschi and Alessandro Cilardo, the authors propose a solution to enable remote IP licensing and activation mechanisms by preserving the full anonymity of the end user, i.e., making it impossible for the Activation Server (AS) in charge of distributing the IP core license to track the user’s behavior across the SoC lifecycle.

Manufacturing testing of two different emerging memory technologies, namely the Thermally Assisted Switching-Magnetic Random Access Memory (TAS-MRAM) and the Resistive Random Access Memory (RRAM) is considered in “An Automated Test Equipment for Characterization of emerging MRAM and RRAM arrays” by Alessandro Grossi, Cristian Zambelli, Piero Olivo, Paolo Pellati, Michele Ramponi, Christian Wenger, Jéremy Alvarez-Herault and Ken Mackay. The authors present a test equipment for their fast characterization. The method can be potentially adapted for any other non-volatile memory generation.

Manufacturing testing is also considered in “Scan-Chain Intra-Cell Aware Testing” by Aymen Touati, Alberto Bosio, Patrick Girard, Arnaud Virazel, Paolo Bernardi, Matteo Sonza Reorda, and Etienne Auvray, where the authors present an evaluation of the effectiveness of different test pattern sets in terms of ability to detect possible intra-cell defects affecting the scan flip-flops. The analysis is then used to develop an effective test solution to improve the overall test quality.

In closing, we wish to thank the reviewers for the quality of their reviews, which have greatly improved the quality of the final submissions for this issue. We thank the authors for their patience through all the stages of the review process, which has been sometimes long. We are grateful to Prof. Fabrizio Lombardi, Editor-in-Chief of these IEEE Transactions on Emerging Topics in Computing, for making this special issue possible.

Sincerely,

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Guest Editors