ADVANCED BIPOLAR CIRCUITS: A PERSPECTIVE

C. T. Chuang

IBM Research Division, T. J. Watson Research Center
Yorktown Heights, NY 10598, U. S. A.

ABSTRACT

This paper reviews the recent advances in high-speed low-power bipolar circuits. The basic underlying principles for achieving superior power-delay performance and load driving capability, such as charge-buffering, dc/ac-coupled active pull-down schemes, and complementary push-pull approaches, are examined. The utilization and combination of these basic principles to form various high-speed low-power npn-only and complementary bipolar circuit configurations are discussed.

I. INTRODUCTION

High-speed bipolar circuits have long been the main stream for high-performance main-frame computer systems. In recent years, the high-end logic has been shifting from transistor-transistor logic (TTL) to emitter-coupled logic (ECL), current-mode logic (CML), and non-threshold logic (NTL) with ECL being the predominant circuit technology. On the other hand, TTL is gradually finding its place in high-end mainframes designed due to its low power-delay product [1-3]. For both ECL (Fig. 1(a)) and NTL (Fig. 1(b)) circuits, the power dissipation has long been known to limit their VLSI applications. The power/speed limitation of both circuits comes primarily from the passive resistors in the delay path where the pull-up delay is limited by the collector load resistor $R_c$ and the pull-down delay is limited by the emitter-follower resistor $R_{ef}$.

This paper reviews the recent advances in high-speed low-power bipolar circuit approaches aiming at achieving superior power-delay performance and load driving capability over the conventional ECL and NTL circuits. In Section II, the basic underlying principles for power/speed improvement such as charge-buffering, dc/ac-coupled active pull-down schemes, and complementary push-pull approaches, are examined. The utilization and combination of these basic principles to form various high-speed low-power npn-only circuit configurations are described in Section III. The cases for complementary circuit configurations are discussed in Section IV. The conclusion of the paper is given in Section V.

II. BASIC PRINCIPLES AND APPROACHES

The most important essence for high-speed low-power operation is the ability to achieve a low standby current while providing a large switching current during the switching transient. While this is easily achieved in CMOS circuits, the bipolar transistors as current controlled devices do not readily offer a similar circuit scheme. The unique property (or problem) of saturation in bipolar transistors further imposes severe constraints on the circuit configurations for high-speed low-power operations.

One approach to overcome these constraints is the use of the charge-buffering principle (Fig. 2(a)). The charge-buffering principle was first used in a complementary circuit configuration [4-6]. The concept utilizes a distinct amount of charge buffered in a charge storage diode (CSD) to generate a large dynamic current for switching while requiring only a very small dc current in standby. This scheme (Fig. 2(a)) basically relies on the use of the large diffusion capacitance of the storage diode as a variable, dynamic capacitor to provide the dynamic current when the input changes. To achieve best performance, the time constant of the charge storage diode must be designed according to the loading and the dynamic capacitance of the driven device. Dynamic to static current ratio of over 100 can be obtained with proper device and circuit designs.

The second approach is to replace the passive resistors with active devices. Applying this to the emitter-follower resistor results in various active-pull-down schemes. The active pull-down element acts like a switch in parallel with a small standby current source (Fig. 2(b)). The switch must be controlled by the logic stage to provide a large transient pull-down current consistent with the logic inputs. While dc-coupling of the switch to the logic stage is preferred, the compatibility of the voltage levels imposes constraint on the available configurations and special device elements may be needed as will be shown later. Ac-coupling, on the other hand, has the advantage of completely blocking the dc signal, thus alleviate the issue of voltage level compatibility, at the expense of introducing capacitors into the circuits and the associated process, qualification, and reliability issues.

Complementary push-pull approaches typically offer the most significant improvement on the power/speed and load driving capability at the expense of complicated process technology. For the most familiar pnp (pull-up) - npn (pull-down) configuration (Fig. 2(c)), both driving devices will saturate if they are also used to set the logical voltage levels (the output is one below $V_{EE}$ or above $V_{CC}$) and the devices have to switch all the way from cut-off to saturation or vice versa. The performance is thus limited by both the saturation and device parasitics (since all the junction and parasitic capacitances have to be charged and discharged). It is possible to use this configuration solely for delivering the large transient current during switching with the logic level set by other means, thus avoiding the saturation problem and improving the performance as will be shown later. For the npn (pull-up) - pnp (pull-down) complementary emitter-follower configuration (Fig. 2(d)), the output voltage always sits half-way between the voltages at the bases of the two transistors in the steady state. In this case, both driving devices are biased at cut-in (nearly on) condition during standby and one of them switches into the active region to provide the switching current. Hence, this configuration avoids saturation and the necessity to charge/discharge the junction/passive capacitance and the switching speed is only limited by the base transit time (diffusion capacitance) of the driving transistors. Notice that in this case, the two base voltages swing in the same direction with equal magnitude except during the switching transient where one of the driving devices experiences base-emitter over-drive.

III. NPN-ONLY ACTIVE-PULL-DOWN CIRCUITS

One example of the dc-coupled active-pull-down circuit is the JFET pull-down ECL circuit (Fig. 3(a)) [7]. This circuit utilizes a 'free' p-channel JFET, which is readily available in any bipolar technology by modifying the base pinch resistor structure, as the pull-down device to replace the emitter-follower resistor $R_{ef}$. The JFET basically acts as a variable resistor whose value is modulated by the gate voltage controlled by the logic stage. The channel resistance is reduced during the output high to low transition to provide a large transient pull-down current as shown by the current-voltage contour in Fig. 3(b). Based on a 0.8 µm double-poly self-aligned bipolar technology [8, 9] at 1.0 mW/gate, the circuit provides about 24% improvement in the pull-down delay for a loaded gate compared with the conventional ECL circuit. To maximize the modulation factor, the doping profile for the JFET channel region may have to be optimized separately from the base region for the npn transistor. Notice that this circuit scheme is straightforward and does not require extra biasing devices/circuit for the pull-down element. However, the leverage of this circuit scheme tends to decrease with reduced voltage swing due to a smaller modulation factor. The leverage also de-
creases as the termination voltage \( V_T \) is raised to reduce the power consumption, again due to a smaller modulation factor. (The current-voltage contour in Fig. 3(b) shifts to the left due to a smaller \( V_C \).

The ac-coupled active-pull-down ECL (AC-APD-ECL) circuit [10, 11] (Fig. 4(a)) utilizes a capacitor to couple a transient voltage pulse to the base of an npn pull-down transistor, thus reducing the dc power consumption in the emitter-follower stage and improving the pull-down delay owing to the large transient pull-down current. The capacitor completely blocks dc signals and alleviates the level compatibility problem. Extra biasing devices are needed to establish the standby current in the output stage. The circuit has also been known as the Turbo ECL circuit and used in 13,000 gate gate array [12]. Notice that in this collector-node ac-coupled scheme, the coupling capacitor represents a load to the logic stage (current switch) and one has to wait until the logic stage switches for the transient signal to be coupled to the pull-down transistor, hence substantial power consumption is still needed in the current switch to achieve fast switching.

The coupling capacitor can be moved from the collector node to the common-emitter node of the switching transistors (Node A in Fig. 4(a)). In this case, the transient current through the capacitor has a speed-up effect on the logic stage. Implementation of this scheme in the NTL circuit results in the so-called SPL (Super Push-Pull Logic) circuit (Fig. 4(b)) [13]. Notice that in this case, it is not necessary to use a separate speed-up capacitor at the common-emitter node of the switching transistors since speed-up effect is already provided by the coupling capacitor.

Charge-buffered coupling (Fig. 2(a)) can also be used to replace the capacitive coupling to eliminate the need for a capacitor, resulting in the charge-buffered active-pull-down ECL circuit (CB-APD-ECL) (Fig. 5) [14]. This charge-buffered coupling scheme provides a much larger dynamic current than that can be realistically obtained through the capacitor coupling. Based on a 0.8 \( \mu \)m double-poly self-aligned bipolar technology at 1.0 mW/gate, the improvement in the loaded delay and load driving capability of the ac-coupled active-pull-down ECL circuit is about 20% (40% for the charge-buffered active-pull-down ECL circuit) compared with the conventional ECL circuit.

IV. COMPLEMENTARY PUSH-PULL CIRCUITS

The combination of the charge-buffering principle and complementary push-pull drivers results in the charge-buffered-logic (CBL) (Fig. 6) [4-6]. The front-end of this circuit resembles the diode-transistor-logic (DTL) except for the use of charge storage diodes. Since the only dc standby current required for the circuit is the sustaining base currents for the pnp (pull-up) and npn (pull-down) transistors, the circuit can operate with extremely low dc current (can be as low as \( \approx 10 \mu \text{A} \)). This circuit hence offers the lowest power-delay product among all the circuits described. The ultimate circuit delay, however, is limited by the heavily-saturated driving transistors.

As mentioned previously, non-saturating pnp (pull-up) - npn (pull-down) circuit configuration is possible as long as the driving devices are not used to set the logical voltage level. One example is the ac-coupled complementary push-pull ECL (AC-PP-ECL) circuit (Fig. 7) which utilizes two capacitors to couple a transient voltage pulse from the common-emitter node of the switching transistors to the bases of a pair of complementary pnp-npn push-pull transistors [15]. In this circuit scheme, the push- and pull-transistor are biased at cut-in condition and one of them is turned on heavily during the switching transient and then back to the cut-in condition, thus providing a high-speed non-saturating push-pull driver. Also notice that during the output low to high transition, most of the pull-up current is supplied by the pull-up pnp transistor \( Q_u \) and only a very small fraction is supplied by the emitter-follower transistor \( Q_E \). The pull-up delay, measured with respect to the time the output voltage crosses the reference voltage, is completely determined by the transient current through \( Q_u \). Thus, the collector load resistor \( R_C \) is decoupled from the delay path and a large resistor, hence a small switching current \( i_{SW} \), can be used without degrading the switching speed. The collector load resistor is used merely for setting the final output voltage level through the emitter-follower transistor \( Q_E \).

Based on a 0.8 \( \mu \)m complementary bipolar process at 0.5 mW/gate, the circuit offers a 2.1X improvement in both the speed and load driving capability for a loaded gate compared with the conventional ECL circuit.

The complementary emitter-follower driver configuration (Fig. 2(d)), when implemented with NTL front-end (Fig. 8), provides a circuit with very strong load driving capability [16]. In this case, an additional emitter-follower transistor \( Q_4 \) is required to drive the base of the pull-down pnp transistor. Based on a 0.8 \( \mu \)m complementary bipolar process at 1.0 mW/gate, the circuit offers a 2.4X improvement in the pull-down delay of a loaded gate and 4.0X improvement in the load driving capability over the conventional NTL circuit. Notice that while the complementary emitter-follower scheme can also be implemented in ECL circuit, the improvement will be less significant because of the front-end configuration (pull-down switching current for ECL versus the case with a current spike in NTL due to the speed-up capacitor) [16].

All the circuits discussed up to now are based on voltage levels as the input and output variables. It is possible to use the current as the input and output variable, as in the case of the complementary current-mirror logic (CCML) circuit (Fig. 9) [17]. This circuit operates primarily by current-mirroring between the input and output stage. The current summation property and the variable output current levels obtainable by changing the current-mirroring ratio provide additional degree of freedom in design. Various logic functions can be implemented simply by changing the current-mirroring ratio as shown in Fig. 9(c) and 9(d). Although in simple circuits, some of the power advantage of CCML over ECL is lost due to the large number of gates needed to implement the function, the additional arithmetic power of the CCML does allow very interesting and compact circuit design in more complex logic applications.

V. CONCLUSION

In summary, while a variety of high-speed low-power bipolar circuits have emerged in recent years, there are some basic underlying principles guiding the development of these circuits. These principles, such as charge-buffering, dc/ac-coupled active pull-down schemes, and complementary push-pull approaches, are examined and the utilization and combination of these principles to form various high-speed low-power npn-only and complementary bipolar circuit configurations are discussed. With a good understanding of these principles and the associated design trade-offs, bipolar circuits will continue to evolve in a performance range unattainable with CMOS circuits.

REFERENCE


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Fig. 1. Schematics of (a) conventional ECL circuit, and (b) conventional NTL circuit.

Fig. 2. Basic high-speed low-power principles and approaches: (a) charge-buffering, (b) dc/ac-coupled active-pull-down, (c) pnp (pull-up) - npn (pull-down) complementary push-pull driver, and (d) npn (pull-up) - pnp (pull-down) complementary emitter-follower driver.

Fig. 3. (a) Schematics of JFET pull-down ECL circuit, and (b) current-voltage contour during transitions: (A) pull-down and (B) pull-up.
Fig. 7. Schematics of ac-coupled complementary push-pull ECL (AC-PP-ECL) circuit.

Fig. 8. Schematics of NTL with complementary emitter-follower driver (NTL-CEF).

Fig. 9. (a) Schematics of complementary current-mirror logic (CCML) circuit, (b) logic symbol (the \( I_{OUT}/I_{IN} \) ratio is shown in the triangular shape), (c) NAND gate (unnormalized output), and (d) NOR gate (unnormalized output).