CHANNEL MOBILITY OF GeSi QUANTUM-WELL P-MOSFET's

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The results of channel mobility of a GeSi quantum-well PMOS from 8 K to 300 K are presented. As the temperature is lowered below 25 K, the field effect channel mobility sharply increases with lowering of the temperature. The mobility at 8 K is found to be 3 times higher than that at 25 K. At very low temperature (~ 10 K), the transition of channel transconductance with gate voltage from a high (GeSi channel) to a low (surface channel) value has been clearly observed.

Introduction

The pseudomorphic growth of lattice mismatched Ge_xSi_{1-x} layers on Si substrates allows the fabrication of many heterostructure devices on GeSi/Si material system. This material system is attractive due to its compatibility with conventional Si processing technology. High performance HBTs and MODFETs have been fabricated on this material system [1,2]. A GeSi PMOS that can perform better than a Si PMOS would be desirable for VLSI applications. This is because for a given current driving capability the p-channel MOSFET occupies 2-3 times more area than that of the n-channel MOSFET. The room temperature operation of a SiO_2/Si/GeSi/Si quantum-well PMOS device has recently been demonstrated by us [3,4]. In this report, we present the measurement results of the channel mobility of GeSi PMOS from 300 K to 8 K. At very low temperatures, a sharp enhancement of channel mobility with lowering of the temperature has been observed. Also, carrier transport with gate voltage from a high-mobility GeSi channel to a low-mobility surface channel has been experimentally found at very low temperatures.

Device Fabrication

The schematic diagram of the MBE grown device structure is shown in Fig. 1(a). Fig. 1(b) shows the equilibrium band diagram of this structure. The Si cap (50 Å), Ge_xSi_{1-x} channel (150 Å), and the setback (100 Å) layers are undoped in order to minimize the coulombic scattering.

GeSi p-channel MOSFET has been fabricated using a conventional Si processing. A 4000 Å LTO is used for field oxide. A thin (36 Å) gate oxide is grown by rapid thermal oxidation of the Si cap layer. B⁺ of 2 x 10^13 cm⁻² @ 20 KeV was used for Source/Drain implant and was annealed at 550 °C for 1 hour followed by a rapid thermal annealing at 800°C for 30 s. Al is used as contact metal and was annealed at 400°C for 20 min.

Results

A 25 µm / 25 µm PMOS is used for all mobility measurements. The field effect mobility is extracted from the peak of the linear transconductance at a drain voltage, V_DS = -0.1 V. The I-V characteristics in Fig. 2 shows good saturation and cut-off behavior at 300 K. The threshold voltage is found to be -1.43 V (Fig. 3) and the room temperature peak low field mobility is 78 cm²/V·s. This low value of room temperature mobility around threshold voltage (~1.43 V) is due to the presence of a large number of interface state charges, which is confirmed by C-V measurements. These interface charges are effective charge centers, and therefore, degrade the mobility at low vertical fields. The device also shows good subthreshold behavior with a subthreshold current slope (S) of 129 mV/decade current. Again, the high value of S is attributed to the interface states which are present either in the as-grown sample or are created during device processing.

Figs. 4 and 5 show respectively the I-V characteristics at 16 K and 8 K. At 16 K, the characteristics show good saturation and cut-off behavior. But below 12 K, the output conducance of the device is found to be high (Fig. 5). At very low temperatures, freezeout causes a large increase in substrate resistance. When the electron-hole pairs are generated at high V_DS by impact-ionization, the electrons flow to the grounded substrate terminal. The IR drop in substrate resistance is shown respectively the I-V characteristics at 16 K and 8 K. At 16 K, the characteristics show good saturation and cut-off behavior. But below 12 K, the output conducance of the device is found to be high (Fig. 5).

The linear transconductance (GM) measurement at 8 K is shown in Fig. 6. The drain current I_D shows two distinct

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slopes with a change over point around -2.9 V. The slope is higher when the magnitude of the gate voltage, VGS, is less than 2.9 V. At this voltage, the channel transconductance changes from a high to a low value showing two different modes of transport. At low value of VGS, most of the carriers will be confined in the GeSi layer, resulting in a high channel mobility. When the magnitude of the gate voltage is increased, the carriers will be mainly concentrated at the Si/SiO2 interface. Thus, a surface channel device is formed and the mobility is reduced.

The channel mobility is extracted from the linear transconductance measurements and the peak field effect mobility is plotted as a function of temperature in Fig. 7. It is found that for temperatures below 25 K, the peak low field mobility rises sharply. The mobility at 8 K is 3 times higher than that at 25 K. This is because the carriers are largely confined to the quantum-well, forming a 2-D hole gas which enhances the channel mobility at very low temperatures.

Summary

We show that a dramatic increase of mobility at very low temperature occurs in GeSi PMOS devices. The transport of the carriers with gate voltage from a high-mobility GeSi channel to a low-mobility surface channel has been clearly observed at 8 K.

References

Fig. 4: I-V characteristics of the device described in Fig. 2 at 16 K.

Fig. 5: I-V characteristics of the device described in Fig. 2 at 8 K ($V_{DS} = -0.1$ V).

Fig. 6: Linear transconductance and drain current as a function of gate voltage of the device described in Fig. 2 at 8 K ($V_{DS} = -0.1$ V).

Fig. 7: Extracted peak channel mobility of the transistor described in Fig. 2 as a function of temperature.

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